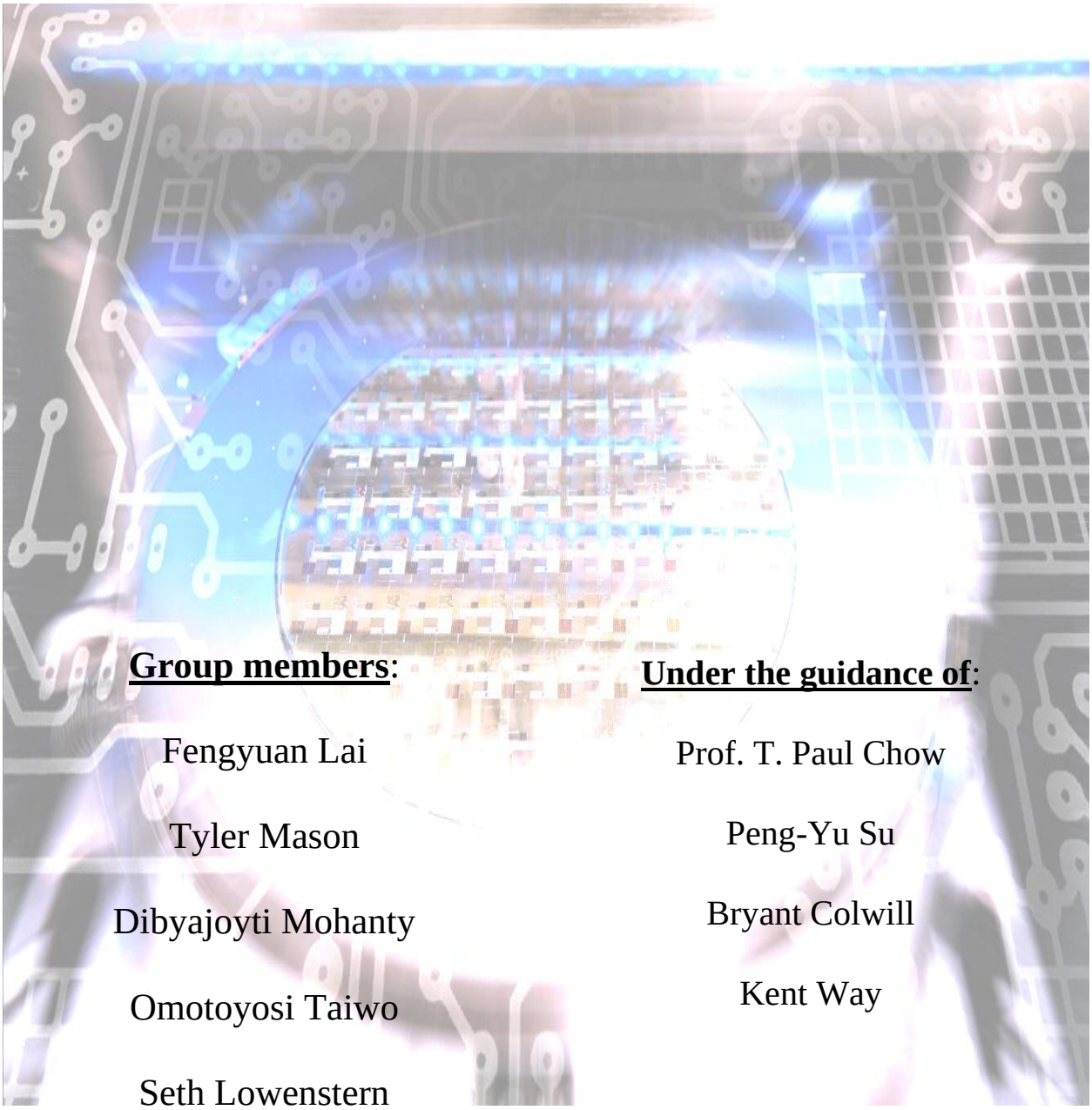
Integrated Circuit Fabrication Laboratory

Final Report – Group 2



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Contents

Table of Figures

Table of Tables

Acknowledgment

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We would like to give a huge thanks to the clean room staff, Bryant Colwill, Kent Way for their guidance and assistance in the IC fabrication process throughout the semester. We learn a great deal from them, which we could never learn from the textbook. A special thanks goes to Zonghuan Lu, who helped us with SEM imaging for failure analysis.

Many thanks go to the teaching assistant, Peng-Yu Su, for his hard work and his help during the fabrication and testing processes.

Abstract

In this Integrated Circuit (IC) Fabrication Laboratory course, we learned the fundamentals of IC fabrication and gained extensive experience in fabricating various types of devices on silicon wafers. In order to fabricate the N-MOS and P-MOS, multiple techniques, including thermal oxidation, photolithography, chemical vapor deposition (CVD), physical vapor deposition (PVD), reactive ion etching (RIE) and ion implantation, were applied during the fabrication process. Film thickness measurements were performed throughout the entire process to ensure that the actual thickness of different layers were with the acceptable error range with respect to the target. The IC fabrication process was also simulated with TSUPREM simulation and the results were compared with our experimental results.

Upon completion of the device fabrication, electrical tests were performed on different types of devices. Current-voltage characteristics were obtained for circular field effect transistors (FETs) and linear FETs on both N-MOS and P-MOS. Leakage current, threshold voltage, transconductance, channel conductance were determined from I-V characteristics. Capacitance-voltage measurements were taken for MOS capacitors. In addition, sheet resistance of source-drain area and contact resistance between metal, source and drain were obtained by characterizing the transmission lines, Kelvin structure, and van der Pauw structure.

Team Responsibility

Group Member	Characterization Responsibilities	Report Contribution
Omotoyosi Taiwo	Transmissionn Lines, Kelvin Structures and Van der Pauw structures for all PMOS and NMOS wafers	-All processing steps (photolithography,etching…) -Transconductance explanation -Contact resistance and Sheet resistance (NMOS,PMOS) -Results from Resistance structure tests -Conclusion All resistance structures
Dibyajyoti Mohanty	-C-V characteristics (Both PMOS and NMOS wafers) -Substrate biasing of PMOSFET and NMOSFETs -Process Modelling	-Device Physics --MOS capacitors, --C-V characteristics --I_D -V_D and I_D-V_G Characteristics -Process Modelling and Simulation for PMOS and NMOS -Electrical Testing --Effect of substrate biasing --On state resistance -- Subthreshold swing --C-V measurement of PMOS -Failure Analysis of PMOS wafers -Conclusion (C-V characterization)

Tyler Mason	-CV characteristics	-Introduction -Introduction to MOSFETS -Transfer Characteristice -Non-ideal MOSFETs -CV Measurements characterization -CV Measurements of NMOS -Conclusion (CV characterization)
Fengyuan Lai	-I-V characteristics for both NMOS and PMOS -Substrate biasing for NMOSFET and PMOSFET	-Abstract and acknowledgment -I-V characteristics -Detailed processing procedures -Conclusion -Report compilation
Seth Lowenstern	-IV characteristics of PMOS and NMOS, including $V_{GS}I_{DS}$, $V_{DS}I_{DS,}$ and extracting parameters -	-Current-Voltage Measurements, NMOS and PMOS -Parallel resistance extraction -Channel Length Modulation -Threshold Voltage -Mathematical device Modeling

1. Technical Background

1.1 Introduction

An integrated circuit, also referred to as an IC, is a collection of electric devices fabricated on a piece of semiconductor material, most commonly silicon. The integrated circuit was first patented by Jack Kilby on February 6, 1959 while employed by Texas Instruments. The IC was an important step forward because it allowed for the miniaturization of electronic components, the most important of which was the transistor.

The first patent for a field effect transistor was filed by Julius Lilienfeld in 1925. Lilienfeld did not publish any research supporting the claims in his patent, nor did he have a working prototype, so his work went ignored until 1947. In 1947, Shockley, Bardeen, and Brattain produced the first practical transistor while working at AT&T's Bell Labs. In 1956 they received the Nobel Prize in Physics for their work "… on semiconductors and their discovery of the transistor effect." In 1960, four years after Shockley, Bardeen, and Brattain won the Nobel Prize, Kahng and Atalla produced the first metal oxide semiconductor field effect transistor, or MOSFET. Transistors replaced vacuum tubes as they are much sturdier, much smaller, and are cheaper and easier to produce on a mass scale.

A transistor itself is an interesting electronic device with applications in signal amplification and binary information switches. This second property makes transistors the basis of modern computing devices. Transistors are capable of these applications because of their unique behavior. A typical MOSFET has three terminals, referred to as the source, gate, and drain. The voltage applied to the gate controls the current between the source and drain, so when no voltage is applied to the gate, there is no current across the source and drain, similar to an open switch. When voltage is applied to the gate current flows and the system behaves as if an open switch had been closed. For lower gate voltages the system shows linear behavior, where the source drain current increases linearly with the gate voltage, which allows the transistor to be used as a signal amplifier.

There is always demand for smaller, more reliable, more efficient electrical devices, which makes the production of integrated circuits, and MOSFETs in particular, is an important topic of study, especially for industry application. In this paper we discuss the production of an integrated circuit on a silicon wafer. The devices fabricated include rectangular MOSFETs, circular MOSFETs, several resistance test structures, and MOS capacitors. These structures were fabricated through the use of multiple techniques, including chemical vapor deposition, physical vapor deposition, photolithography, plasma etching, wet etching, and ion implantation.

In Chapter 1 of this report the theoretical background of the behavior, processing, and testing of IC devices is laid out. In Chapter 2 the actual processes used to fabricate the ICs are described. In Chapter 3 the method by which the devices are tested, and the results of those tests are presented. Chapter 4 compares the results of the actual devices to the behavior of a simulated IC and discusses the differences between ideal and real behavior of the devices.

1.2 Device Physics

1.2.1 Introduction to MOSFET

A metal oxide semiconductor field effect transistor, or MOSFET, is one of the most common devices fabricated as part of an integrated circuit. The transistor is so useful because it allows for the electronic amplification or switching of signals, the second property making it the basis of digital electronics designs.

A MOSFET can either be n-type or p-type, depending on the type of dopant used to create the source and drain terminals. For an n-type MOSFET the device is fabricated on a p doped substrate. The source and drain terminals are created by highly doping the substrate with an n+ dopant. A thin layer of oxide and a layer of metal, for our devices a layer of polysilicon, are fabricated on top of the space between the n+ doped areas, creating the gate terminal. A cross section of a MOSFET is shown in the illustration below.

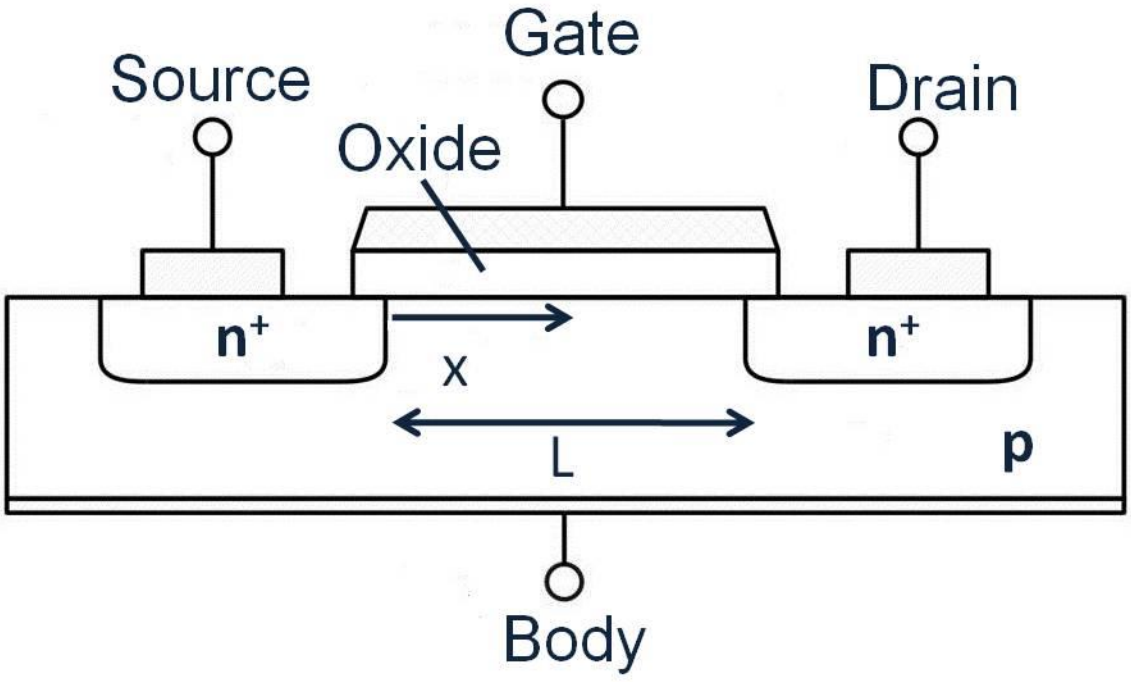

Figure 1.2.1 MOSFET Cross-Section

The MOSFET is operated by the application of a voltage to the gate terminal. The metal and the substrate act as the plates in a parallel plate capacitor, with the oxide being a dielectric medium separating the two plates. Applying a positive voltage to the gate terminal, relative to the substrate, causes the build up of negative charges in the substrate near the oxide-substrate boundary. These negative charges come in the form of a depletion layer and an inversion layer of mobile electrons. The mobile electron layer forms a channel that allows current to flow between the source and drain terminals. The voltage applied to the gate required to form the conducting channel is known as the threshold voltage, and it is an important characteristic value of a MOSFET. The threshold voltage can be controlled in the ideal case by factors such as oxide thickness and substrate dopant concentration. The threshold voltage can also be affected by non-ideal effects due to fabrication methods.

1.2.2 Different Types of Field-Effect Transistors

1.2.3 Basic Device Characteristics

1.2.4 MOS Structure

Metal Oxide Semiconductor (MOS) structure consists of a layer of insulating oxide layer sandwiched between metal and semiconductor, that's why it is also Metal Insulator Semiconductor (MIS) structure. It behaves like a parallel plate capacitor, with the oxide layer working as a dielectric layer and the terminals being the metal and semiconductor. When bias is applied to the top metal terminal, it produces an electric field, which results in collection of charge carriers (majority or minority depending on the polarity of bias) at the semiconductor and oxide interface.

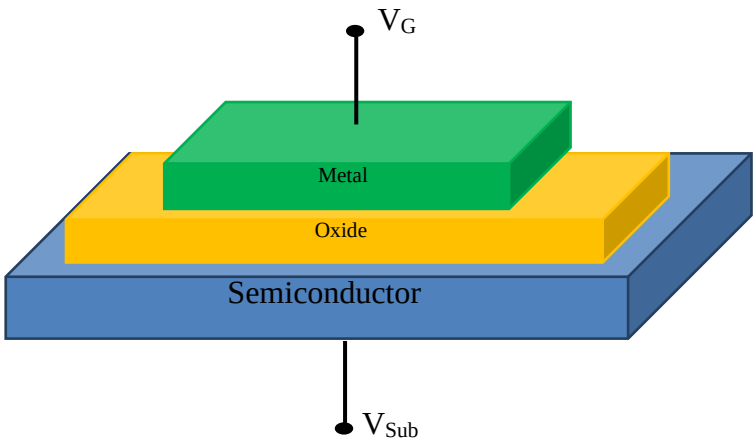

Figure 1.2.2 Metal Oxide Semiconductor (MOS) Capacitor structure- Oxide layer sandwiched between metal and semiconductor layers.

1.2.4.1 Energy Band Diagram of MOS Capacitors

Energy band diagram is used to study carrier behavior at different biasing condition in a semiconductor. In an energy band diagram, the energy difference between Fermi level and Vacuum level is known as Work function (φ) and the energy difference between conduction band of the semiconductor and vacuum level is known as Electron affinity (χ). The work function of metal is denoted as φ_m and that of semiconductor is φ_s. If under zero bias condition the Fermi levels of semiconductor and metal are aligned with each other ($\varphi_m = \varphi_s$), then it is called Flat Band condition. The behavior of MOS structure under different biasing conditions has been discussed below.

1.2.4.1.1 Under zero bias condition (V_G=0)

The energy band diagram of ideal p- and n- MOS structures under zero bias condition is as shown in Figure 1.2.3. For our analysis, let us consider a p-type semiconductor MOS structure. As it is flat band condition ($\varphi_{ms} = \varphi_m - \varphi_s = 0$), the Fermi levels are perfectly aligned with each other and there is no charge flow in the structure.

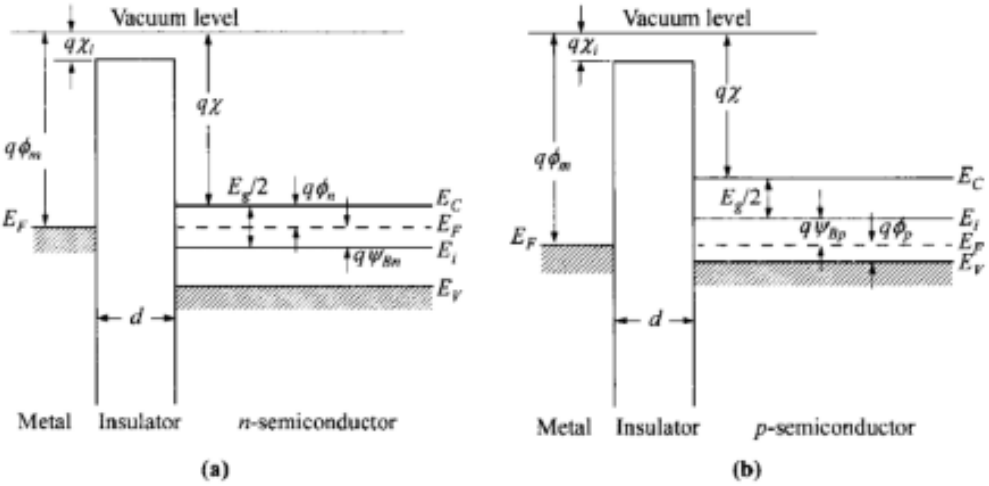

Figure 1.2.3 Energy band diagrams of ideal (φ_{ms} = 0) p- and n-MOS structure under zero bias condition [1].

1.2.4.1.2 Under negative bias condition (V_G<0)

When a negative bias V<0 is applied to the metal with respect to the semiconductor, the metal becomes negatively charged and an equal amount of positive charge or hole accumulates at the semiconductor-oxide interface. This is known as accumulation condition and it results in a storage of majority carriers at the interface. Due the application of this bias, Fermi level of metal (E_{Fm}) moves above the semiconductor Fermi level (E_{Fs}) by an amount qV. Due to this shift, band bending occurs as shown in the Figure 1.2.4.

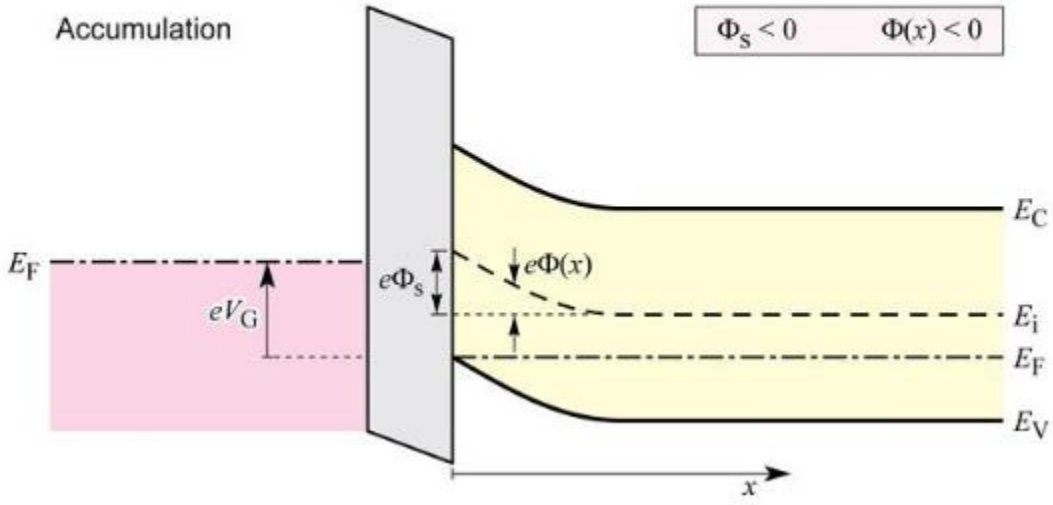

Figure 1.2.4 Band Structure of NMOS Capacitor in Accumulation condition where $V_G < 0$ [2].

1.2.4.1.3 Under small positive bias ($V_T > V_G > 0$)

When a small positive voltage is applied to the metal, it becomes positive with respect to the semiconductor, hence the accumulated holes at the interface are dispersed back into the bulk. This step is known as Depletion as it involves depletion of majority carriers from the interface. So in this stage the balancing negative charge at the interface is due to the immobile acceptor ions. Due to the positive potential applied to the metal, the Fermi level for metal, E_{Fm} shifts below E_{Fs} causing a band bending opposite to the previous step.

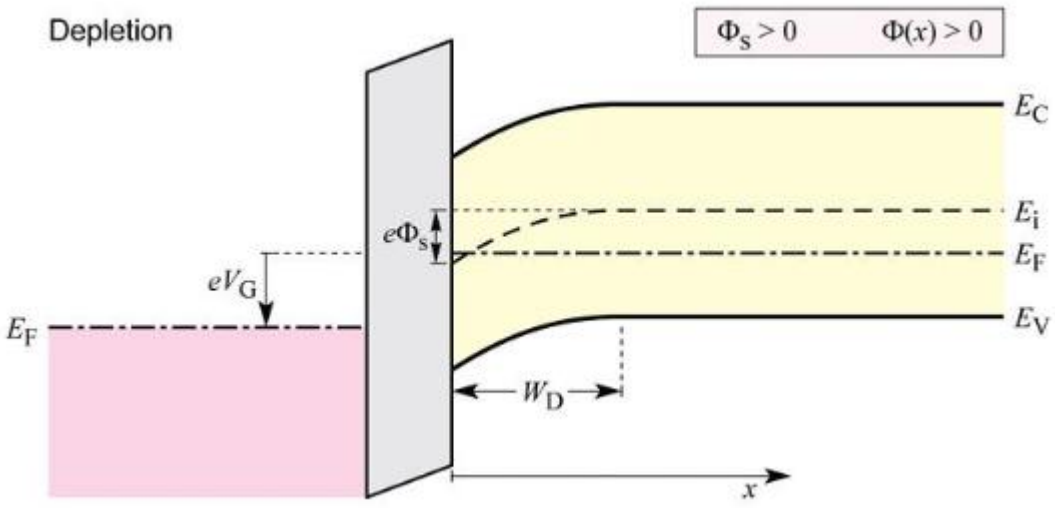

Figure 1.2.5 Band Structure of NMOS Capacitor in Depletion regime, where applied voltage $V_T > V_G > 0$ [2].

1.2.4.1.4 Under large positive bias ($V_G > V_T$):

When the positive bias applied to the metal electrode exceeds a certain voltage (known as Threshold Voltage V_{th}), to compensate the positive charge, electrons start piling at the interface. As the minority carrier concentration accumulated at the interface exceeds that of majority acceptor ions, inversion is said to occur as shown in Figure 1.2.6. The intrinsic energy level (E_i) bends further below the Fermi level. At Threshold voltage, onset of inversion is said to occur at which,

$$\varphi_s = 2\varphi_F = \frac{2(E_{i(bulk)} - E_F)}{q}$$

Where, φ_F is the electrostatic potential of Fermi level with respect to the intrinsic level for p-type substrate, given by

$$\varphi_F = \pm \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)$$

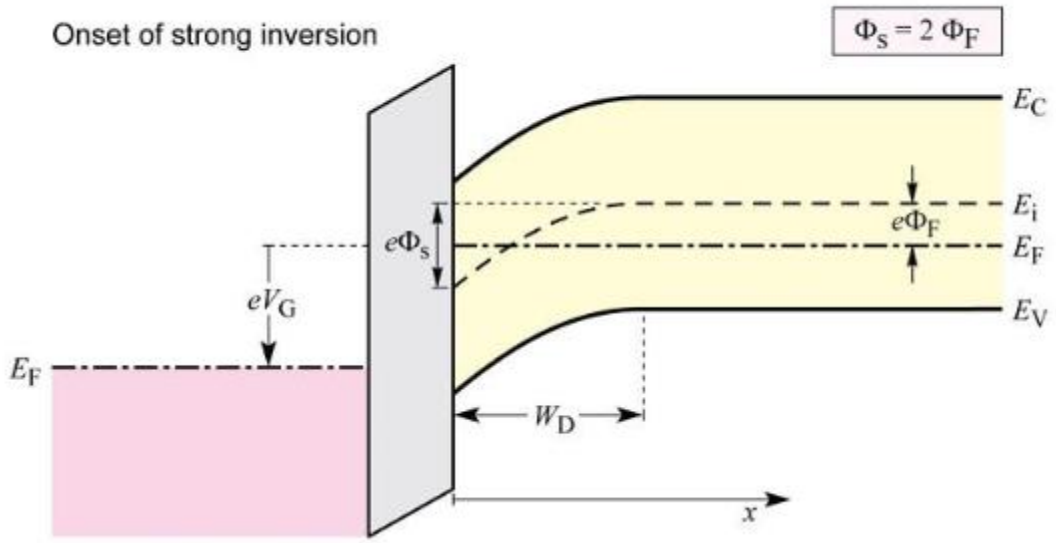

Figure 1.2.6 Band Structure of NMOS Capacitor at the onset of Strong Inversion regime with applied voltage to the metal electrode $V_G = V_T$ [2].

For n-type substrate, the negative sign is used with N_A replaced by N_D. If the voltage is increased way beyond threshold voltage, the depletion width doesn't change anymore. So the maximum depletion width for NMOS is given by,

$$W_{Dmax} = \sqrt{\frac{2\varepsilon(2\varphi_F)}{qN_A}} = 2\sqrt{\frac{\varepsilon kT}{q^2 N_A}\ln\frac{N_A}{n_i}}$$

The voltage drop across a MOS capacitor is given by,

$$V_G = V_{ox} + \varphi_s$$

Where, V_{OX} is the voltage drop across the oxide and φ_s is the surface potential of the semiconductor. So at the onset of strong inversion, when the voltage across the capacitor is the threshold voltage, the above equation becomes for an NMOS,

$$V_{th} = 2\varphi_F + \frac{\varepsilon_s x_{ox}}{\varepsilon_{ox}}\sqrt{\frac{4qN_A}{\varepsilon_s\varepsilon_0}\varphi_F}$$

The same equation for PMOS,

$$V_{th} = 2\varphi_F - \frac{\varepsilon_s x_{ox}}{\varepsilon_{ox}}\sqrt{\frac{4qN_D}{\varepsilon_s\varepsilon_0}(-\varphi_F)}$$

Surface potential φ_s can be used to define various biasing cases,

1) $\varphi_s < 0$, Accumulation of holes (Accumulation regime)

2) $\varphi_s = 0$, No band bending (Flat band condition)

3) $\varphi_s > 0$, Hole depletion from interface (Depletion regime)

4) $2\varphi_F > \varphi_s > \varphi_F$, electrons start piling at interface, (Weak inversion regime)

5) $2\varphi_F >> \varphi_s$, electron inversion layer formed (Strong inversion regime)

The perpendicular electric field in depletion region is given by:

$$E_x = \frac{\sqrt{2}kT}{qL_D}\sqrt{\left[\left(e^{\frac{-q\varphi_x}{kT}} + \frac{q\varphi_x}{kT} - 1\right) + \frac{n_{p0}}{p_{p0}}\left(e^{\frac{q\varphi_x}{kT}} - \frac{q\varphi_x}{kT} - 1\right)\right]}$$

Where, φ_x is the potential at any point at a distance x from the surface and L_D is the Debye screening length given by,

$$L_D = \sqrt{\frac{\varepsilon_s kT}{q^2 p_{p0}}}$$

Using Gauss's law at the surface, charge stored at the surface can be determined by, $Q_S = -\varepsilon_S * E_S$, where E_S is the electric field at the surface (x = 0). The plot of Q_S in terms of surface potential φ_s, is given in Figure 1.2.7 below, which also shows the various bias regimes.

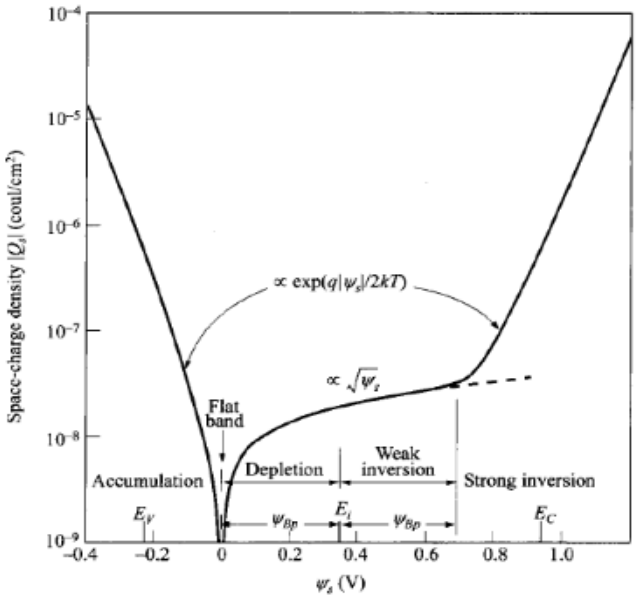

Figure 1.2.7 Variation of surface charge density Q_S as a function of surface potential ψ_S for a p-type Si substrate with $N_A = 4 \times 10^{15}cm^{-3}$ [1].

1.2.4.2 MOS Capacitance-Voltage (C-V) Characteristics:

The voltage applied across the MOS structure drops across it and is given by,

$$V_{MOS} = V_{OX} + \varphi_S$$

Where, V_{MOS} is the voltage applied across MOS, V_{OX} is the voltage drop across the oxide and φ_s is the surface potential of the semiconductor. The equivalent circuit for a MOS structure has two capacitors in series with each other- voltage independent oxide capacitance and voltage dependent depletion capacitance. There is variation in MOS capacitance depending on applied voltage and frequency is shown in Figure 1.2.8.

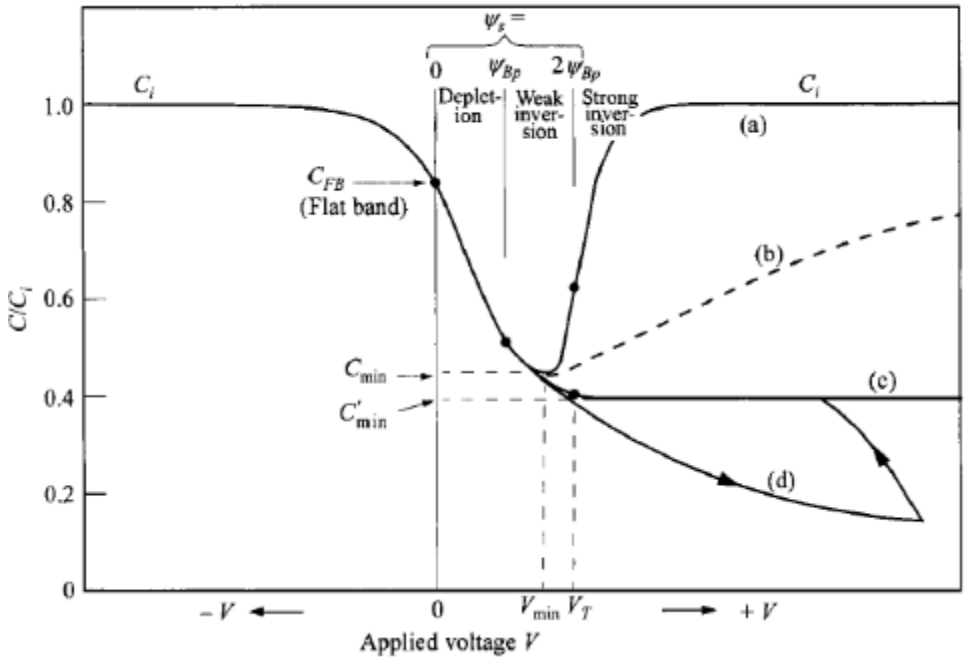

Figure 1.2.8 Capacitance-Voltage characteristic of an NMOS with various bias regimes- accumulation, depletion, weak inversion, strong inversion and deep depletion indicated on the curve [1].

1.2.4.2.1 Accumulation Capacitance

In Accumulation regime ($V_G < V_{FB}$), the negative voltage applied to the NMOS causes accumulation of holes at the interface. The high capacitance is close to the oxide capacitance. The oxide capacitance per unit area is given by,

$$C_i = \frac{\varepsilon_{OX}}{d}$$

Where, d is the oxide thickness and ε_{OX} is the oxide permittivity. It is denoted by C_i on the left hand side of Figure 1.2.8.

1.2.4.2.2 Depletion Capacitance

When the voltage is increased beyond V_{FB}, and positive charge added to metal plate, repels the accumulated holes from semiconductor and oxide interface exposing the negatively charged acceptors. As the voltage is increased further, to compensate for the increasing positive voltage on the gate, the depletion layer thickness increases and holes from the interface are gradually removed. So the depletion regime capacitance is the series combination of oxide and depletion capacitances, which is given by,

$$C = \frac{C_i C_d}{C_i + C_d}$$

Where, $C_d = \frac{\varepsilon_s}{W}$ is the depletion capacitance.

1.2.4.2.3 Inversion Capacitance

As the voltage is further increased and threshold voltage is reached, the charge on the surface of semiconductor changes from positive to negative and a layer of electrons get deposited. This inversion layer formation also results in maximum depletion layer width. Any further increase in gate voltage, doesn't cause subsequent increase in depletion layer width. Hence the capacitance in inversion region is the series combination of oxide capacitance with minimum depletion capacitance resulting from maximum depletion width. It is given by,

$$C = \frac{C_i C_{dmin}}{C_i + C_{dmin}}$$

Where, $C_{dmin} = \frac{\varepsilon_s}{W_{max}}$ is the minimum depletion capacitance.

1.2.4.2.4 Frequency Dependence

Also the C-V curve of a MOS capacitor is frequency dependent. At high frequency, beyond the Threshold voltage (V_{th}), the minority carrier generation and recombination is not quick enough to oscillate quasi-statically with the frequency variation. Hence the capacitance saturates beyond the threshold voltage for high frequency. But if the frequency of the applied bias is low enough, the minority carrier generation can provide enough carriers to the semiconductor interface with increasing voltage. Hence the capacitance increases again in the inversion region before saturating as shown in Figure 1.2.8.

1.2.4.2.5 Deep Depletion Mode

If the rate of increase of applied voltage on gate is large enough, the capacitance continue to decrease beyond the threshold voltage too. This is caused by continual increase of the depletion layer thickness beyond the threshold voltage as the minority carriers are not able to meet the increasing positive potential on the gate. This mode is known as Deep Depletion mode.

1.2.5 Current-Voltage Characteristics

MOSFET is a four terminal Device with four terminals as Source, Drain, Gate and Substrate. For an n-channel MOSFET, when the gate voltage (V_G) exceeds threshold voltage (V_T), an inversion layer of electrons is formed at the semiconductor surface forming a conducting channel in between source and drain. When a positive drain voltage is applied in this condition, the MOSFET starts to conduct. Source and Substrate terminals are usually shorted to ground potential. The conduction of MOSFET can be divided into three regimes, e.g. linear regime, onset of saturation regime and strong saturation regime.

- **Linear regime ($V_G > V_T$ and $V_D < V_G - V_T$):**

  In this region a conducting channel of electron is formed for gate voltages higher than the threshold voltage. The channel formed behaves like a resistor and with increasing positive voltage applied to the drain, it starts conducting. The drain current increases linearly with drain voltage in this regime, so it is called linear region in the output characteristics of a transistor. However, the voltage drop as well as the depletion region in the source and drain increases with increase in drain voltage and weakens the inversion layer as shown in Figure 1.2.9(a).

- **Onset of Saturation regime ($V_G > V_T$ and $V_D = V_G - V_T$):**

  With increase in drain voltage, the depletion width increases in drain and source region and progressively narrows the channel width. Because of the voltage drop, the gate voltage varies from V_G at source to $V_G - V_D$ at drain. When $V_G - V_D = V_T$, then the channel near drain becomes narrowest and the pinch-off is said to occur as shown in Figure 1.2.9 (b).

- **Strong Saturation regime ($V_G > V_T$ and $V_D > V_G - V_T$):**

  With further increase in drain voltage, the pinch-off point moves closer and closer to the source-end and the pinch of region widens. This region has high resistance and little carriers. The electrons are attracted from the source region into the channel and are drifted across the pinch off region by strong longitudinal electric field present in the region as shown in Figure 1.2.9 (c). In this region, a change in drain voltage, doesn't cause a significant increase in drain current, hence it is called the saturation regime.

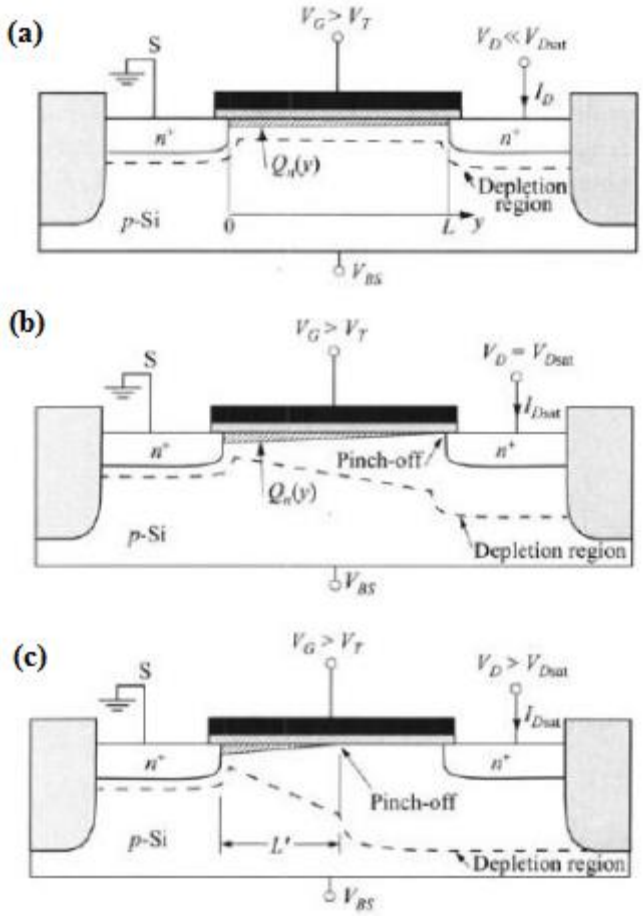

Figure 1.2.9. NMOSFET in various operating conditions, (a) linear regime, (b) onset of saturation and (c) Strong saturation regime [1].

1.2.5.1 Output Characteristics (I_D vs. V_D):

An ideal I_D vs. V_D characteristics of n-channel MOSFET is as shown in figure below. The channel contains mobile charge carriers whose charge is given by,

$$Q_n = -C_i(V_G - V_T - V_x)$$

Where, V_G is the applied gate voltage, V_D is the applied drain voltage and V_x is the voltage at a distance x from the source. The conductance of a differential element dx in channel is given by, $\mu_n Q_n(x) Z dx$, where μ_n is the surface mobility, Z is the channel width. Drain current is obtained by integrating the conductance over the channel given by,

$$\int_0^L I_D dx = \int_0^{V_D} \mu_n Z |Q_n| dV_x$$

Which gives the expression of resulting drain current to be,

$$I_D = \frac{\mu_n Z C_i}{L}\left[(V_G - V_T)V_D - \frac{{V_D}^2}{2}\right]$$

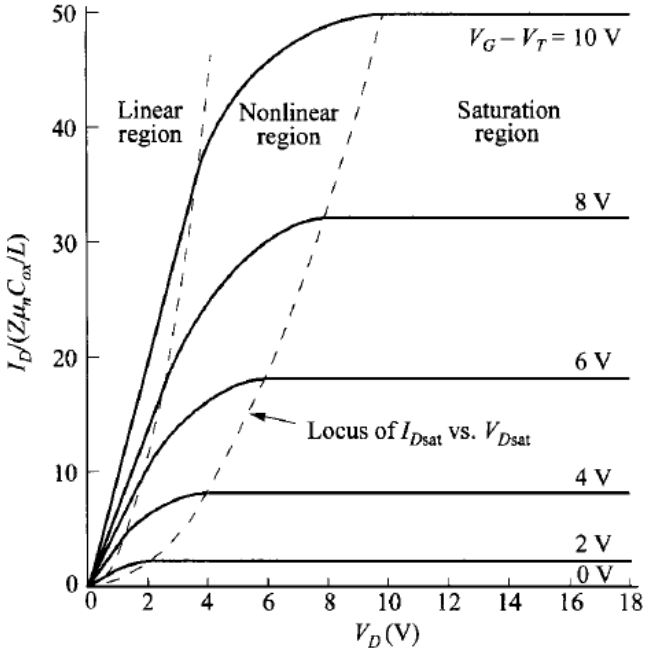

Figure 1.2.10 Ideal I_D-V_D characteristics of an NMOSFET with dotted lines separating the linear region, non-linear region and saturation region from each other [1].

The conductance can be of two types-

a. Channel Conductance (g_d): It is the rate of change of drain current with respect to drain voltage at constant gate voltage. It can be determined from the slope of the output (I_D-V_D) characteristics. It is given by:

$$g_d = \left|\frac{\partial I_D}{\partial V_D}\right|_{V_G}$$

b. Transconductance (g_m): It is the rate of change of drain current with respect to gate voltage at constant drain voltage. It can be determined from the slope of transfer (I_D-V_G) characteristics. It is given by:

$$g_m = \left|\frac{\partial I_D}{\partial V_G}\right|_{V_D}$$

I_D -V_D relationship in different regions of output characteristics can be given by:

1. Linear region:

   The relationship is linear in this region at $V_D << V_G - V_T$, given by:

$$I_D = \frac{\mu_n Z C_i}{L}\left[(V_G - V_T)V_D - \frac{{V_D}^2}{2}\right]$$

   and transconductances are given by:

$$g_d = \left|\frac{\partial I_D}{\partial V_D}\right|_{V_G} \cong \frac{\mu_n Z C_i}{L}(V_G - V_T)$$

$$g_m = \left|\frac{\partial I_D}{\partial V_G}\right|_{V_D} \cong \frac{\mu_n Z C_i}{L} V_D$$

2. Onset of Saturation region:

   The relationship in this region where $V_{D(sat)} = V_G - V_T$

$$I_{D(sat.)} \cong \frac{\mu_P Z C_i}{2L}(V_G - V_T)^2 = \frac{\mu_P Z C_i}{2L}\left(V_{D(sat.)}\right)^2$$

   and transconductances are given by:

$$g_d = \left|\frac{\partial I_D}{\partial V_D}\right|_{V_G} \cong 0$$

$$g_m = \left|\frac{\partial I_D}{\partial V_G}\right|_{V_D} \cong \frac{\mu_n Z C_i}{L}(V_G - V_T)$$

1.2.5.2 Transfer Characteristics

The transfer characteristics of a device are expressed as a curve of drain current as a function of gate voltage, while drain voltage is held constant. There are two characteristic regions of the transfer characteristics curve, the linear region and the saturation region. In the linear region the drain current changes linearly with the gate voltage. The linear threshold voltage is found through finding a linear fit for the linear region. The x-intercept of the fit is the linear region threshold voltage, and the slope of the fit is the transconductance of the device.

As the gate voltage is increased the system enters the saturation region and the transfer characteristic curve begins to show parabolic behavior. It is helpful to plot the square root of the drain current as a function of gate voltage to examine this region. Taking a linear fit of this region in the square root of drain current plot allows us to extract the threshold voltage for the saturation region.

1.2.6 Non-ideal MOSFET

Theory is very informative on how a device can be expected to behave, but it is very difficult to fabricate a device that shows actual ideal behavior. There are multiple different effects that contribute to non-ideal behavior in a MOSFET device.

Work Function Difference:

In the ideal case we assumed that the work function of the metal gate was identical to the work function of the silicon dioxide. This is not going to be true in any real device. The difference in work functions will cause a shift in the threshold voltage, making it non-ideal.

Mobile Charge:

Highly diffusive species, such as Na^+ and K^+, are likely to be present in the oxide as contaminants introduced during fabrication. These contaminants change the threshold voltage off the device.

Fixed Charge:

The production of the oxide layer usually leaves excess ionic silicon at the interface between the silicon and the oxide. These 'dangling bonds' are usually formed when the oxidation process is ended abruptly. These fixed charges cause a shift in the flatband voltage of the device.

1.2.7 Additional Effects in MOSFETs

1.2.7.1 Short channel effect

Short –channel effect is a consequence of scaling down MOSFET sizes. When a FET is small enough such that the channel length is the same order of magnitude as the depletion-layer widths of the source and drain junction. The short channel effect modifies the threshold voltage thereby altering the performance of the FETs.

The short channel effect can be attributed to 2 physical causes; the limitation due to the electron drift characteristics in the channel and the modification of the threshold voltage that occurs from shortening the channel length. The following are the 5 short channel effects that have been observed to occur

- Drain-induced barrier lowering and punchthrough
- Surface scattering
- Velocity saturation
- Impact ionization
- Hot electrons

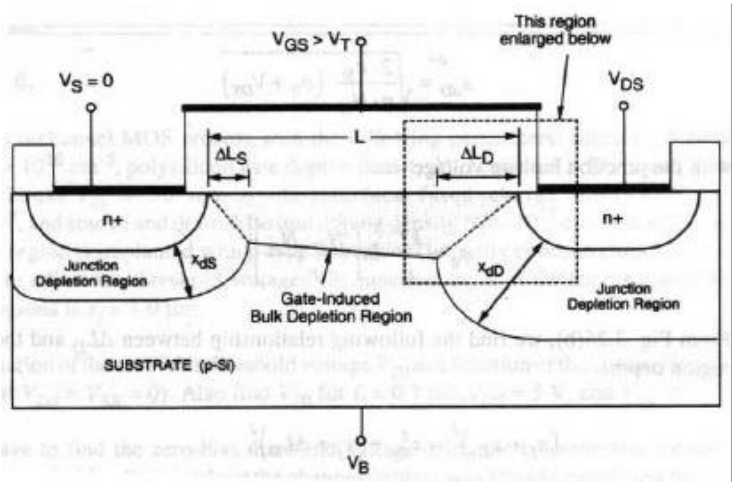

Figure 1.2.11 Simplified geometry of a short channel FET

1.2.7.2 Drain –Induced barrier lowering

This is one of the consequences of short channel effect. When the channel is not long enough, the depletion layers of the drain and the source merge and punchtrough occurs. Current can only flow when an inversion layer has been created by applying bias at the gate. If this gate bias is not large enough to invert the surface, the electrons (or holes) form a barrier that blocks flow in either direction. This can be corrected by increasing the gate voltage. But in small channel devices, drain to source bias also affects this barrier, therefore when the drain voltage is in-

creased it leads to the Drain-Induced barrier lowering effect. This means the threshold voltages can be reached at lower gate voltages because the drain voltage is contributing to the threshold voltage value, which it normally shouldn't.

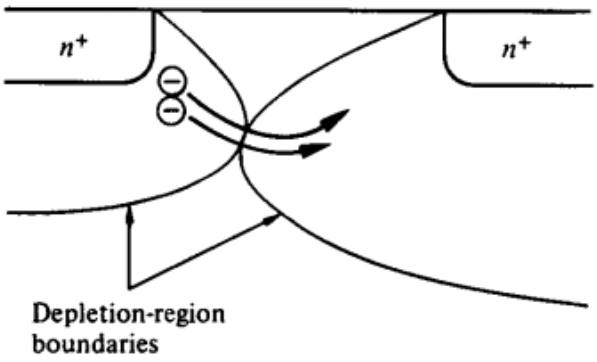

Figure 1.2.12 Punchthrough between source and drain.

The solution of this is to make shallower junctions, thinner oxides or longer channels.

1.2.7.3 Substrate bias effect

The substrate bias effect also known as the body effect is the modification of device threshold voltage through the application of bias on the substrate (body) of the device. The depletion layer is affected by the voltage difference between the source and the bulk (body). The change in threshold voltage is given by

$$\Delta V_T = \frac{\sqrt{2\varepsilon_S q N_a}}{C_{OX}}\left(\sqrt{2\phi_F + V_{SB}}\right) - \sqrt{2\phi_F}$$

where V_{SB} is the bulk-to-source voltage. A change in VSB would therefore cause a corresponding shift in the threshold voltage. The body is sometimes referred to as "second gate" because of the effect it has on the threshold voltage and how it can turn on or off the transistor. The way to

combat this is to set a fixed body bias voltage and that way the body voltage is always constant and is no influenced by device doping

1.3 Basic Processing Steps for MOSFETs

Fabrication of devices includes basic processes like Photolithography, Ion implantation, Oxidation, Etching, Diffusion, Material Deposition, and Metallization. Due to increasingly small device dimensions, keeping impurities out of the fabrication process is one of the driving forces behind processing innovation and techniques. Majority, if not all are carried out in pristine contaminant free environment, known as clean rooms The one where the processing of these wafers took place was a 100 rating clean room which is the number of 0.5Um impurities per cubic feet. The different scales of clean room can be seen below in Table 1.3.1. The 1 rating clean- room is a little difficult to measure however.

Table 1.3.1 Clean room rating by air purity

Rating	Number of 0.5um particles per cubic feet	Number of 5-um particles per cubic feet
10,000	10000	65
1000	1000	6.5
100	100	0.65
10	10	0.065
1	1	0.0065

In industry, most of the processes are automated, and devices orders of magnitude smaller, smallest consumer ready transistor size is Intel's 22nm technology, are being manufactured. The importance of precision and even less contamination is worth millions. Wafer uniformity is important and contaminants affect device performance in unpredictable ways. Impurities can affect critical parameters like threshold voltage (Vth) which needs to be the same or have minimal percentage error, if they are to be used in the same top level circuitries.

Sources of contamination usually include, organic materials from humans, which can introduce extra charges to the devices, thereby affecting parameter like electron/hole mobility. The

processes listed above would be discussed in detail below. These are the key steps required to make a functional MOSFET and through mask manipulation other structures like transistors, capacitors, van der pauw structure, Kelvin structures are made. These are important in the characterization of the MOSFETs.

1.3.1 Wafer Cleaning:

Wafer cleaning is usually done using the RCA clean. This is important for the removal of organic contaminants, ionic contaminants, and in some cases thin oxide film.

RCA Clean:

The first step is to remove all the organic materials by dipping the wafers in a heated ammonium hydroxide (NH4OH), Hydrogen Peroxide (H2O2), and Deionized (DI) water solution using a ratio of 1:1:5 respectively. A pre-solvent clean, using acetone can be done, but not necessary. During this step the solution removes organic residues and also oxidizes the silicon and leaves a thin oxide layer on the surface of the wafer.

The next step is a quick dip in a HF and water solution with ratio of 1:50 respectively at 25oC to remove the thin oxide layer that was caused by the previous step. This is done for a very short time because the solution reacts quickly. Safety precaution must also be taken by wearing protective gear due to the dangerous nature of the chemicals being handled.

The last step is done to remove ionic contaminants which may have been introduced in the previous steps. The wafer is dipped in a solution of Hydrochloric acid (HCl), H2O2 and DI water using a ratio of 1:1:5, respectively.

The wafer is cleaned using a quick dump rinser (QDR) using deionized water, after every step to prevent the chemicals used in that step from reacting with the ones in subsequent steps. Finally it is dried and cleaned because water can easily attract floating particulates if left on the surface.

Piranha Solution:

Another cleaning method is piranha etch, which contains a mixture of sulfuric acid (H2SO4) and H2O2. This is a strong oxidizing agent however, and leads to formation of oxide on the wafer surface.

The solution must be handled extra cautiously because it is an exothermic reaction and releases heat of over 100oC. This high temperature may cause vigorous boiling and splashing of extremely toxic solution. It must be allowed to cool reasonably before applying any heat.

This method is mostly used to clean photoresist residue from the silicon wafers. The equation below is the mechanism of operation of this solution. The product, H2SO5 (Caro’s acid) is the key component that vigorously dehydrates the residues in the manner of which piranhas feed; hence the name Piranha solution.

1.3.2 Thermal oxidation:

The ability of silicon to form SiO2 is the major reason why Si is the dominant material used for the fabrication of MOSFETs. The oxide serves as a diffusion barrier during impurity diffusions, protection for the p-n junctions formed due to the presence of source and drain wells in the substrate, insulating film to separate different levels of devices, as isolation structure, and passivation layer.

Two types of oxides can be formed based on the uniformity of the atomic configuration. Fused silica is amorphous SiO2 which is the oxide we are interested in based on the arrangement of atoms in the molecule. The other type of SiO2 that can be formed is known as Quartz.

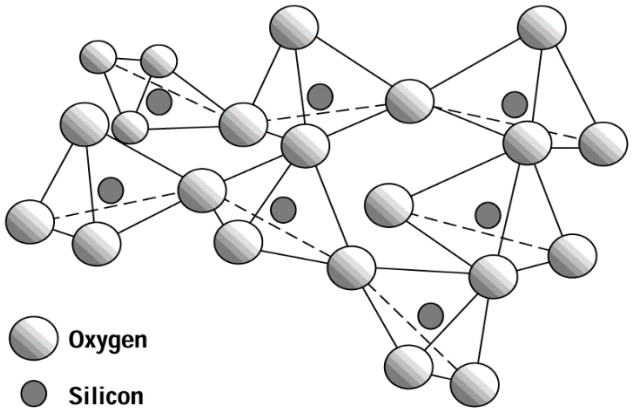

Figure 1.3.1 Physical structure of SiO2

Oxidation can be done either by using pure oxygen (dry oxidation), or water vapor (wet oxidation). They both have their pros and cons and depending on the application of the oxide either or both can be used to form SiO2. Oxidation is done at really high temperatures, between 700 – 1300 oC and is therefore referred to as Thermal oxidation. Dry oxidation is slower but produces lower quality oxide, whereas wet oxidation is faster but produces poorer quality oxide. Wet oxidation is faster because the solid solubility of (OH) in SiO2 surface is several orders of magnitude higher. The mechanism for dry and wet oxidation can be seen below:

$$Si_{(s)} + O_{2(g)} \text{ --> } SiO_{2\ (s)} \text{ - Dry oxidation:}$$

$$Si_{\ (s)} + 2H2O\ (g) \text{ --> } SiO2\ (s) + 2H2\ (g) \text{ - Wet oxidation:}$$

The thickness of oxide produced during oxidation needs to anticipated and accounted for when determining the thickness of the substrate. This is because the oxide eats some of the silicon wafer to produce the oxide, and that's usually around 46% of the thickness of the final oxide layer.

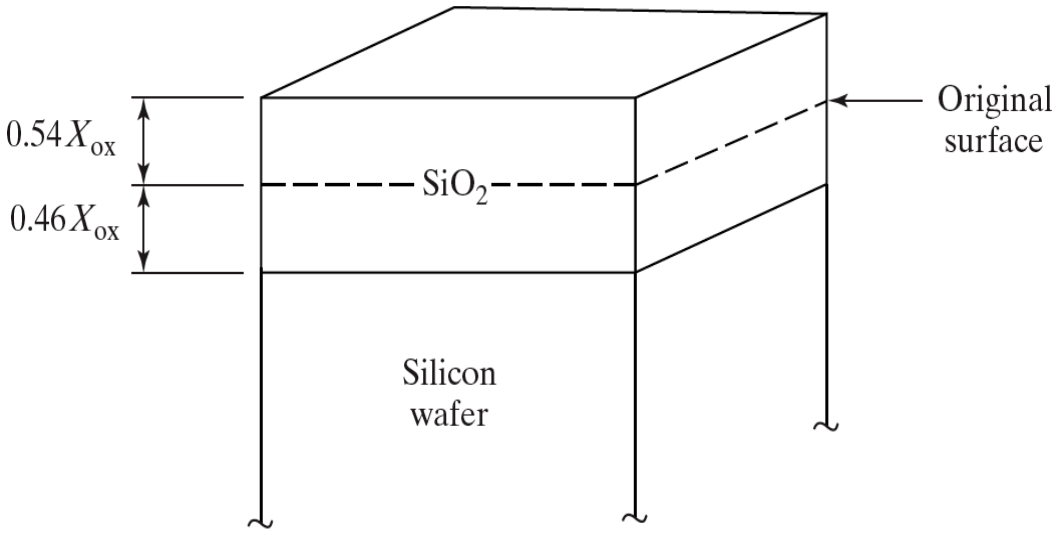

Figure 1.3.2 Final Si surface after oxidation

The oxidation process takes longer with more time because the diffusing species need to travel through increasing thickness of the oxide layer to reach the silicon and form SiO2.

Reaction Kinetics:

The final thickness of oxides grown can be calculated by knowing the initial concentration of oxygen at the Si-SiO2 interface, conc. in the reacting species and the flux (flow of oxygen molecules). The equation derived from these is

Xo = 0.5A((1+4 B/A^2 (t+ tau))^0.5 -1). T = Xo^2/B + Xo/(B/A) - tau

Tau = Xi^2/B + Xi/(B/A).

Where Xo = final oxide thickness, D = diffusion coefficient, N = concentration of oxygen, Xi = initial oxide thickness tau = initial time required to grow initial oxide, t = time elapsed. A and B are constants that vary with temperature, D, N, and pressure. B/A is called the linear rate constant and B is called the parabolic rate of oxygen through the oxide. B/A is more important for small oxide thicknesses and the thickness increases with time linearly, hence linear rate constant. The longer the time, however the thickness increases with the square root of time, hence parabolic rate constant. If the time is long enough, the thickness (Xo) can be estimated be Xo^2 = Bt.

Table 1.3.2 Linear and Parabolic rate constants for dry and wet oxidation

TABLE 3.1 Values for Coefficient D_0 and Activation Energy E_A for Wet and Dry Oxygen*

	Wet O_2(X_i = 0 nm)		Dry O_2(X_i = 25 nm)	
	D_0	E_A	D_0	E_A
<100> Silicon				
Linear (B/A)	9.70×10^7 μm/hr	2.05 eV	3.71×10^6 μm/hr	2.00 eV
Parabolic (B)	386$\mu m^{2]}$/hr	0.78 eV	772μm^2/hr	1.23 eV
<111> Silicon				
Linear (B/A)	1.63×10^8 μm/hr	2.05 eV	6.23$\mu 10^6$μm/hr	2.00 eV
Parabolic (B)	386μm^2/hr	0.78 eV	772μm^2/hr	1.23 eV

*Data from Ref.[9]

Effects of oxidation:

Oxidation causes the redistribution of impurities in Si, because some of the impurity species prefer to occupy oxide, while some prefer to occupy the silicon. This would usually cause of pile up of the species near the Si-SiO2 interface.

Other effects of oxidation include the formation of interface charges, oxide fixed charges, oxide trapped charges, and mobile ionic charges. These need to be properly controlled because they can have adverse effects on the MOSFET parameters like threshold voltage and breakdown voltage. Chlorine can be added during oxidation to remove these fast moving impurities.

1.3.3 Photolithography

Photolithography (sometimes called UV lithography or optical lithography), is the process of transferring patterns of geometric shapes on a mask to a thin layer of photosensitive material covering the wafer. These patterns are used to define various regions of integrated circuits

This is one of the key processes in MOSFETs fabrication, because it allows for the creation of extremely small patterns with precise controls due to the use of light wavelength. It has been predicted to die out a long time ago, but due to tricks and innovation, the semiconductor industry can transfer features on the order of 0.07um. The steps involved in Photolithography include:

Deposition of Barrier Layers:

The first thing to do is deposit barrier layers like Si3N4 or SiO2. Like mentioned above the most common barrier layer used is SiO2, and this can be deposited using thermal oxidation. A barrier layer can also be a metal in some special devices.

Spin coating:

Spin coating is done to deposit thin films on flat substrates. Before putting the photoresist, Hexamethyldisilazane (HMDS) is applied to aid the adhesion of the photoresist to the substrate. This is spun for uniformity and then slowed down or fully stopped to apply the photoresist. This is done by applying a small material (photoresist) on the center of the wafer, and then rotating it at a really high speed again, thereby spreading the resist by the centrifugal force generated. The spinning is usually done between 20 to 80 revolutions per second for 45 to 60 seconds.

Soft bake (Pre bake):

This is done to drive off excess photoresist solvent and improve adhesion, typically at 90 o 100oC for a minute on a hot plate. The typical layer thickness after spin coating is between 0.5 and 2.5 um, and although soft baking increases this thickness a little, this increase can be ignored.

Mask alignment:

Mask or photomask is a computer designed layout on a glass plate that allows light to shine through some parts and set predefined patterns on a wafer. The mask has to be aligned perfectly, usually through the use of machines. Most devices require a large number of masks and layers, and the lower layers need to be considered when aligning masks

Pattern exposure:

After the mask has been aligned, the photoresist is exposed to UV usually between 0.2 – 0.4 um wavelength. Other sources can be used like Argon Fluoride (ArF) or Krypton fluoride (KrF) laser sources. The light reacts with the photoresist depending on the type of resist used. If a positive photoresist is used, the unexposed area becomes harder to remove leaving that pattern on the wafer. On the other hand, negative photoresist hardens the exposed area. The positive resist is a solution of an alkali soluble resin, a photoactive dissolution inhibiter and a solvent. The negative resist is a photosensitive compound which hardens on exposure to light, by forming cross-linked polymer molecule. Negative resists can however cause problems due to swelling and this limits resolution which is why positive resist is more widely used. There are 3 basic methods of exposure:

Contact printing: this is when the mask touches the surface of the wafer and usually results in very high resolution projections, as small as 0.5um features can be transferred. The disadvantage to this is that, due to the mask is touching the wafer, any damage to the wafer will cause the mask to be damaged and disrupt all the mask alignments that follow.

Proximity printing: There is no physical contact between the mask and the wafer in proximity printing which causes less damage to the mask, but limits the resolution that can be achieved. Resolution ranges between 2um and 4um.

Projection printing: This is the most widely used exposure method in the industry today; it can achieve very small resolutions less than 1um and eliminate mask damage. The basic idea is to take a small part of the mask, scan that and project it on the wafer. This can be done differently; using scanning projection aligners, reduction with step and repeat process, and non-reduction with step and repeat process. These processes have advantages but the drawback is that it requires a high degree complexity and takes longer.

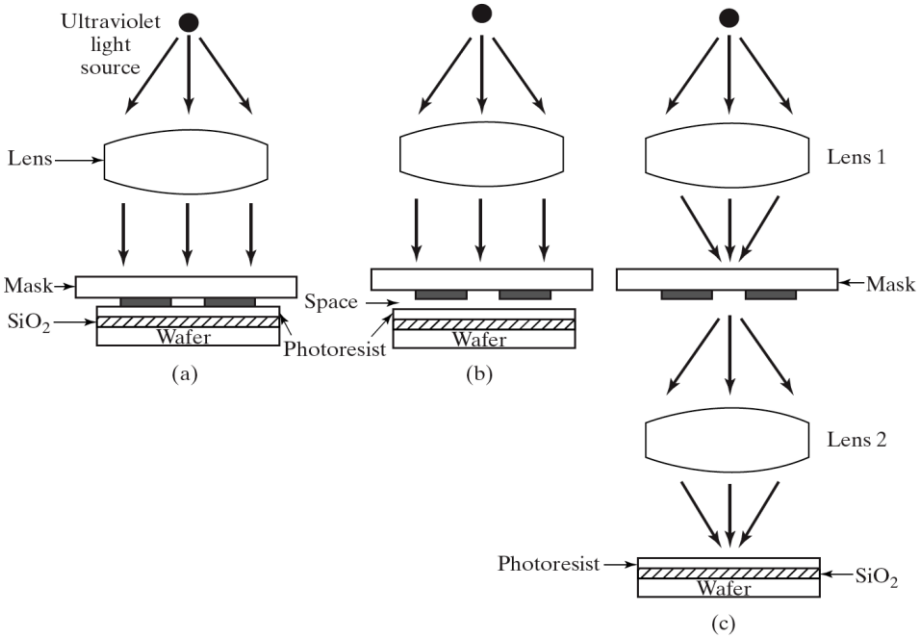

Figure 1.3.3 Three basic methods of exposure

Resist Development:

The resist is developed by dipping the wafer in developing solution, which removes some of the photoresist depending on whether positive or negative resist has been used.

Hard bake and Window etch:

This step is done to harden the photoresist. This is usually done to help reduce the standing wave phenomenon that is caused by interference patterns of the light sources used. The hard baking is also done to make the resist more durable and be able to work as a protective layer to prevent ion implantation, or etching procedures that would be done later in the process from affecting the layers beneath it.

Photoresist removal:

When the resist is no longer needed, it is removed from the wafer using a stripper. This solution breaks the adhesion bonds between the wafer and the resist. This can also be done by oxidizing the resist, this method is known as ashing.

1.3.4 Material deposition

For many of the steps involved in fabricating MOSFETs, thin films are usually required to be deposited one time or the other. Unlike thermal oxidation that is a reaction between Si and an oxidizing agent, physical deposition of thin films doesn't usually eat into the silicon, because it is just a layer of another material being physically put on the wafer. The material could be further moved into the substrate through diffusion or ion implantation. Depending on the nature of the film being deposited, it could be done using physical processes or chemical processes, which is similar in mechanism to oxidation.

Chemical vapor deposition (CVD):

This is used to deposit various films such as Polysilicon, SiO2, Si3N4 and tungsten.

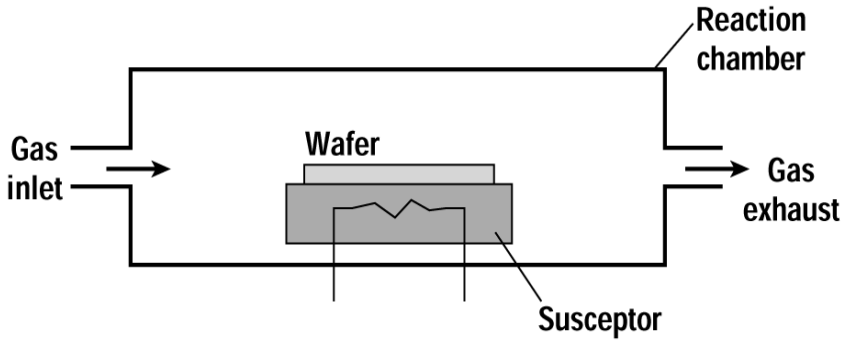

Figure 1.3.4 Simple CVD system

There are 4 types of CVD; atmospheric-pressure CVD (APCVD), hot-wall low pressure CVD (LPCVD), parallel-plate plasma-enhanced system, and photo-enhanced (PECVD) system:

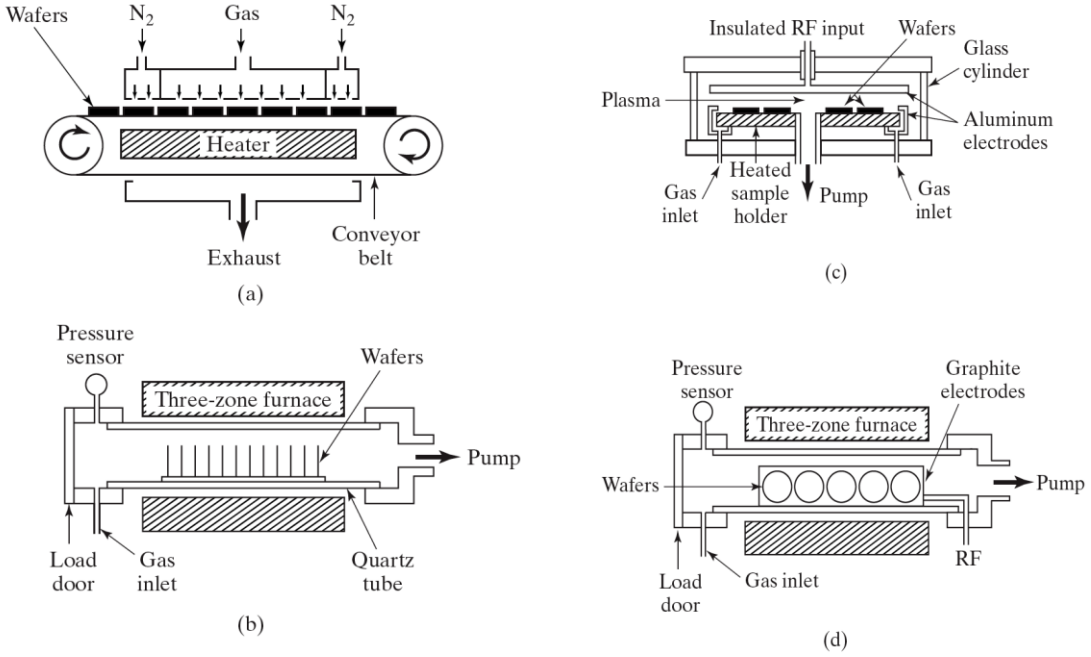

Figure 1.3.5 (a) APCVD (b) LPCVD (c) parallel-plate (d) PECVD systems

CVD works by pumping gasses into a reactor which contains the wafer. The gasses that enter the chamber then react together to form a layer of material on the substrate, or sometimes they react with the surface of the material. The quality of the film deposited depends on the type of material that is put in the chamber and the type of reaction that occurs. The reaction could either be homogeneous or heterogeneous. Homogenous reactions occur in the gas phase, therefore require higher pressure. The material produced is not usually uniform and can result in dusting (e.g. snow formation). Heterogeneous reaction however takes place on the surface, and usually require lower pressure and temperature. This is results in a better quality film deposited.

Physical Vapor Deposition (PVD):

The two major types of physical deposition include Evaporation and Sputtering. These are more suitable for devices with larger dimensions where film quality is not of utmost importance, but cost and high yield is required. Metal deposition is carried out mainly by PVD.

Evaporation: The metal is melted in a vacuum and transported to the sample through the vacuum. This is process that is slowly being phased out of Silicon fabrication technology. A typical evaporation system can be seen below:

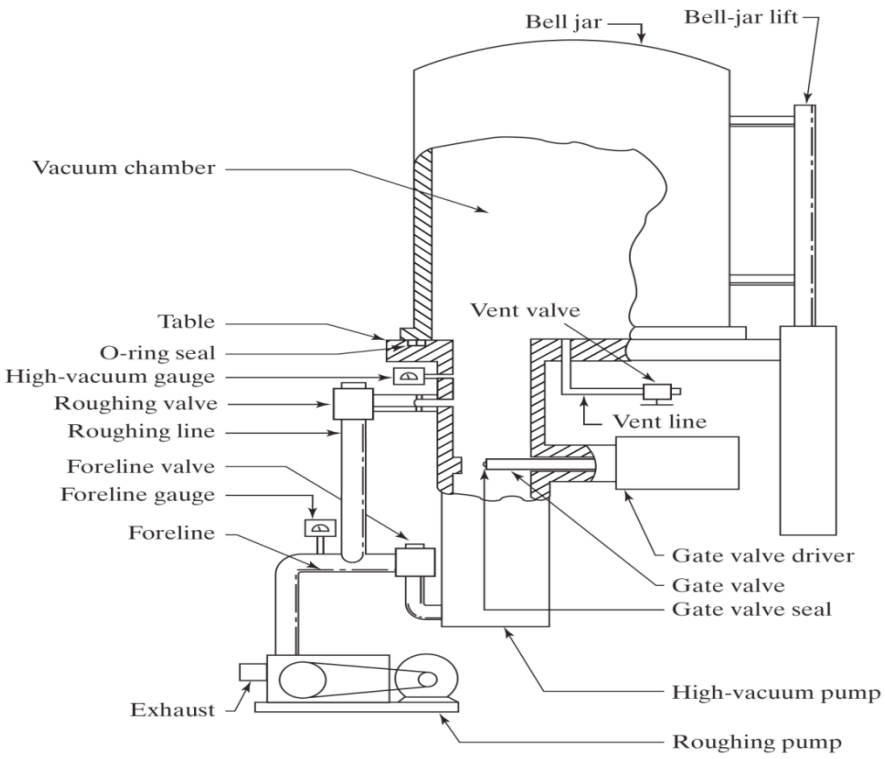

Figure 1.3.6 Typical evaporation vacuum

Evaporation is done in a high vacuum to allow the vapor to reach the substrate without reacting with other gas-phase atoms in the chamber, and to reduce impurity contamination.

Sputtering: This is the primary alternative to evaporation, because it results in better step coverage then evaporation. It also causes less radiation damage than in the case of e-beam evaporation. The wafer and target are usually kept in the same chamber to maximize deposition. This is achieved by accelerating ions towards the surface of a target, which causes the source material to disassociate from the target in vapor form and condense on the wafer surface. This usually takes place in vacuum with low pressure and temperature

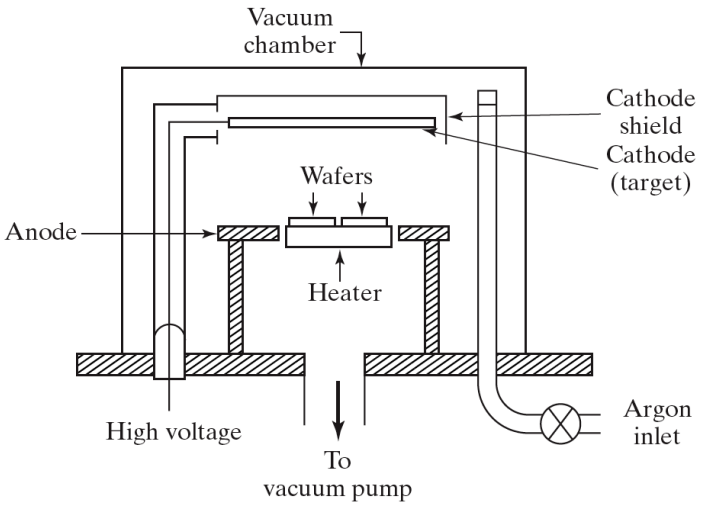

Figure 1.3.7 Sputtering chamber

1.3.5 Etching

Etching is done to transfer the image in a mask and photoresist to the underlying layer of the devices. This process can also be used to remove surface damage after mechanical polishing by smoothening the surface and to expose crystal defects that are present. There are 2 main methods of etching:

Wet chemical etching:

Chemical etching uses liquid etchants to remove materials on wafers. The wafer must de dipped into the solution, and most times agitated (temperature, or just shaking) to allow uniform etching. Wet etching usually lacks anisotropy (directional etching) but it is very selective because it is a chemical process. This is because the etchant only reacts with the material that it is trying to remove. Wet etching is a less destructive method of etching but lacks process control, especially for dimensions less than 2 um. A lot toxic waste is also produced.

Oxide etching: The most common solution used to etch SiO2 is HF and water with a composition ratio of 1:6 respectively. This solution doesn't etch silicon, and rate of etching is also dependent on the density of the oxide layer, which is a good indicator of the quality of the oxide. Thermal oxide etches at a rate of approx. 1200Ao/min but CVD oxide etches at a rate of approx. 3000Ao/min. The etching chemical reaction can be seen below:

SiO2 + 6HF -> H2+ SiF6 + 2H2O (SiF6 dissolves in water)

The etch rate decreases with time because the reaction consumes HF, therefore a buffering agent like ammonium fluoride (NH4F) is usually added. This allows the HF concentration in the solution to remain the same

Silicon etching: silicon is commonly etched with nitric acid (HNO3), HF and water solution. This is almost a 2 in 1 process because the nitric acid is an oxidizing agent which oxidizes the silicon, and as mentioned above, the HF etches any SiO2 that is formed. The etch rate is very because the quality of oxide produced is not very good which makes the HF acid attack it faster. Below is the mechanism involved in Si etching:

Si+HNO3+6HF----> H2SiF6+HNO2+H2+H2O

Dry plasma etching:

Dry plasms etching is done by producing energetic free radicals, neutrally charged, that react at the surface of the wafer. This process is the more commonly used one in VLSI technology. Wet chemical etching is not good for device dimensions of less than 2um because there is a lot undercutting of the mask due to the isotropic (in all directions) nature of wet etching. Dry plasma etching has a lot of advantages over wet etching apart from the obvious reason that it can be used for small dimension devices. Dry etching preserves Photoresist (PR) unlike wet etching acids which etch a little of the PR layer. There is much better control, less sensitivity to temperature and very little or no toxic waste generated. However, there are still trade-offs because the possibility of damage is increased due to the energetic particles that bombard the wafers. The common gasses that are used for dry etching include CFCl3, CFCl2, CF3C, CF4, CHF3, C2ClF5. The chemical reaction can be seen below:

$$Si + 4F \rightarrow SiF4 - \textit{Si etching}$$

$$(CF)x + SiO2 \rightarrow SiF4\ (CO + CO2\ \text{etc.})$$

$$SiO2 + 4F \rightarrow SiF4 + O2 - \textit{2 step SiO2 etching.}$$

1.3.6 Ion implantation

This is a method of introducing dopant species into a substrate that uses highly energetic beams of ions are accelerated in an electric field and impacted onto a solid which modifies the physical, chemical and electrical properties of the wafer. It is sometimes used as an alternative to pre-deposition before diffusion which is explained below. This is a very attractive alternative because it allows for more precise process control, depth control and can be used to implant a wide dosage range from 10^11 – 10^16 cm^-2 and is also insensitive to native surface contamination. Ion implantation is also useful as a method of introducing gettering sites inside wafers, enhancing compound formation kinetics or as an isolation technology. The main disadvantages of ion implantation include damage to the wafers, sputtering contamination, cost, and channeling.

The process is usually carried out at low temperatures and typically has ion energies of 10keV-200 keV and even up to 1MeV for special applications. Junction depths are typically in the 100 Ao – 0.5um range. An ion implantation system can be seen in Fig. xx .

The dopant source is usually a compound that is ionizable, e.g. BF3, B2H6, and PH3 etc. electrons collide with the dopants to form ionized particles which are then accelerated using a 50 – 500kV source. The ions then move into the mass separator where a magnet is used to control the trajectory of these ions. The scanner uses electrostatic or electromagnetic means to raster beam across a wafer.

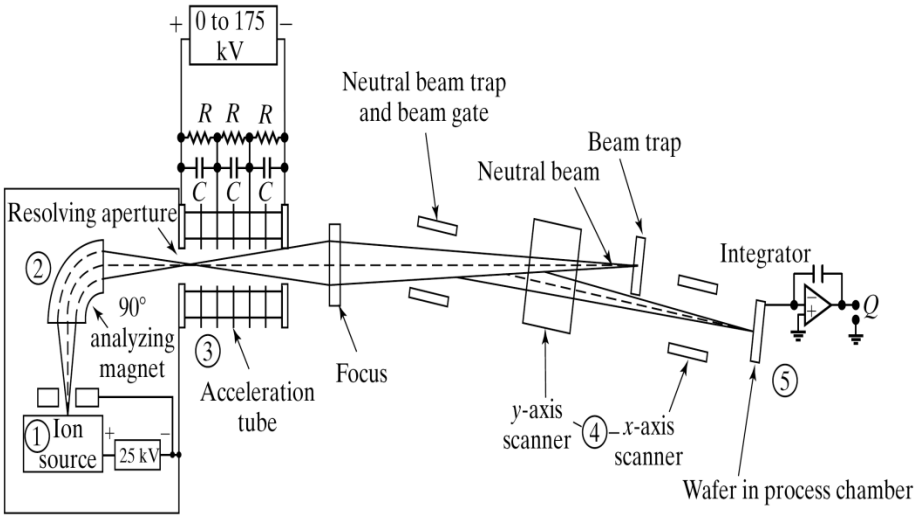

Figure 1.3.8 Ion implantation system

The depth of the implanted specie can be calculated using the Range Theory, which uses energy loss mechanisms to predict the depth of implanted atoms. By taking into account nuclear collisions that lead to energy loss, crystal damage, and angular deflection the junction depth can be estimated.

1.3.7 Diffusion

Diffusion plays an important role in the fabrication of devices. Diffusion is used to form n and p type regions in the wafer by introducing dopants, which causes the region to have more electrons (n-type) or holes (p-type). Like in most maerial physics, any material that is free to move will experience a net redistribution in response to concentration gradient. This is evident in processes like diffusion, osmosis, etc. Materials tend to naturally want to be in equilibrium. The movement of material is and can be modelled using Fick's first law of diffusion. The flux (flow) of the diffusing is given by

$$J = -D\, dN(x,t)/dx.$$

Where D is the coefficient of diffusion and dN/dx is the concentration gradient. By applying continuity equations using Fick's second law of diffusion, a differential volume, in addition to

concentration is also taken into consideration when modelling the diffusion of species across gradients.

J2-J1/deltax = dJ/dx.

Diffusion rate is not however entirely dependent on just the flow rate alone however. Because diffusion is a physical process by which atoms wander through a lattice, the rates are also dependent on other factors like host lattice, defect features, temperature, etc. Diffusing species occupy host species using three different mechanisms.

Interstitial diffusion: Also known as lattice diffusion, in this process, thermal agitation causes the guest atom to hop from void to void in the host molecule and eventually come to rest due to loss of energy. The dopant specie does not however replace the host atom at the lattices.

Substitutional diffusion: the guest atom moves from vacancy to vacancy throughout the crystal lattice. In this mechanism, the host atoms are replaced across the lattice structure.

Diffusion is highly dependent on temperature, and the junction depth can be modelled depending on the type of diffusion being done. It could be constant source diffusion or limited source diffusion. In constant source diffusion, the concentration of the diffusing species is kept constant throughout the process, whereas in limited source diffusion a certain amount of required dose is pre implanted and then diffused into the substrate.

1.3.8 Interconnections and contacts

This is also known as metallization because the materials usually used are almost exclusively metals, because they serve as electrical connections from the device to the outside world. These contacts are sometimes referred to as Ohmic contact and the point of this is to serve as a means of getting current into and out of the device, therefore we typically want our ohmic contacts to have very low resistivity, low chemical interactivity and mechanically strong.

Commonly used materials include Al, Ti, W, Cu, and in some special caes Ni, Platinum and Pala dium. Below is a table of the bulk resistivities of commonly used metals

Table 1.3.3 Bulk resistivity of commonly used metals

Metal	Bulk resistivity (uOhm-cm)
Silver (Ag)	1.6
Aluminum (Al)	2.65
Gold (Au)	2.2

Cobalt(Co)	6
Copper(Cu)	1.7
Molybdenum(Mo)	5
Nickel (Ni)	7
Palladium (Pd)	10
Platinum (Pt)	10
Titanium (Ti)	50
Tungsten (W)	5

The effectiveness of the metal as an ohmic contact can also depend on the doping of the substrate, for instance Al tends to form an ideal ohmic contact with p-type substrates, whereas it can sometimes form a Schottky barrier diode with n-type substrates. Aluminum is the most commonly used metal contact, whereas Cu is more commonly used for interconnects. As can be seen from the table above, these 2 metals have the lowest resistivity and would transfer current the best.

There are problems that could occur during this step, for instance aluminum spiking can occur due to Si being absorbed into the aluminum. These can lead to junction shorting or current leakage. Electromigration can also occur due to the presence of high current densities which causes voids to form and an electron wind can cause the movement of metal atoms.

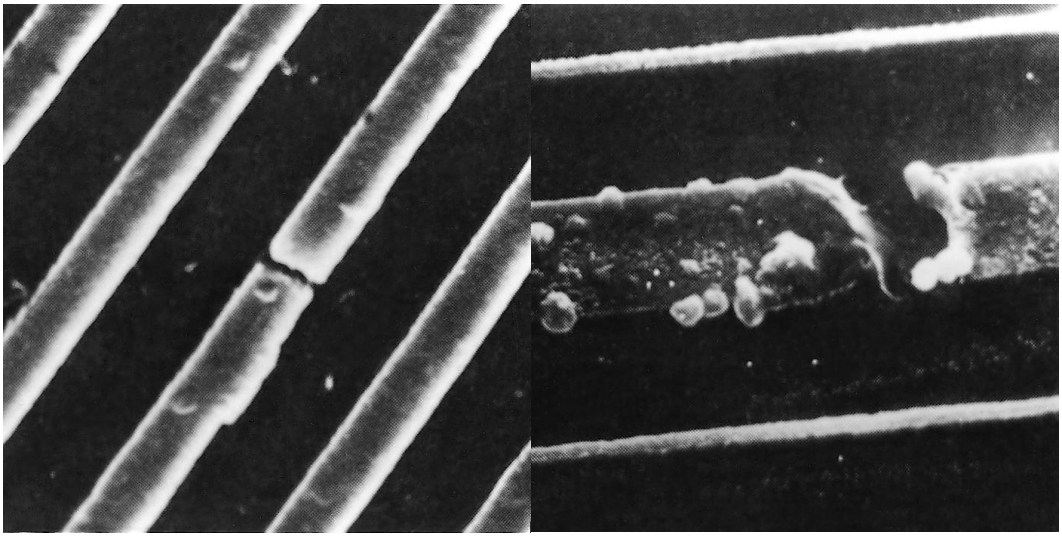

Figure 1.3.9 SEM images of failure due to interconnections

1.4 Process Modeling

TSUPREM4 is an important process simulation tool to simulate and predict the device behavior to a fair amount of accuracy. The same procedure and processing steps were used for simulation as for the real devices. After the complete process simulation some electrical characteristics were also simulated.

The substrate used for process simulation for NMOS is a p-type <100> Si substrate doped with Boron at 2E15cm^{-3}. The process simulation was divided into multiple steps, such as: (1) Field oxide growth and patterning, (2) Gate oxide, Poly Si growth, S/D formation and implantation, (3) ILD and metal deposition. The various steps along with the code used for them are given below:

1.4.1 NMOS Process Simulation

1.4.1.1 Mask Definition

Mask file was created to simulate a MOSFET of channel length of 4µm. The scaling factor used for the mask is 1000, i.e. 1000 units on the grid is equivalent to 1 µm. The mask file defines 5 different mask types, such as: Field, Gate, Poly, Contact and Metal.

Mask File:Mask1.tl1

```
TL1 0100
/Channel length =4um
/Scaling factor = 1000
/
1000
-5000 5000
5
Field 2
-5000 -4000
4000 5000

Gate 3
-5000 -4000
-2000 2000
4000 5000

Poly 1
-2000 2000

Contact 4
-5000 -3750
-2260 -600
600 2260
3750 5000
```

Metal 3
-3960 -2200
-1400 1400
2200 3960

1.4.1.2 Field Oxide Growth and Patterning:

Field oxide of a thickness of 1 µm was grown on top of the p-type Si substrate and then it was patterned using lithography to expose a region of 8 µm in the center. This region is known as the active area of the device. For field oxide growth a combination of dry and wet oxidation steps were followed. The TSUPREM4 code for the program is given below along with the patterned field oxide cross-section.

Code for Field oxide growth and patterning:

```
$Field oxidation and patterning

$ Define the grid

MESH GRID.FAC=1.5

$ Read the mask definition file

$MASK IN.FILE=Mask1.tl1 PRINT GRID="Field,Poly"

MASK IN.FILE=Mask1.tl1 PRINT GRID="Field,Poly"

$ p-type substrate initialization

INITIALIZE <100> BORON=2E15 I.RESIST=10


$Field oxide growth

Diffusion temp=400 time=90 t.final=1000 N2

Diffusion temp=1000 time=60 N2

Diffusion temp=1000 time=30 dryO2

Diffusion temp=1000 time=300 wetO2

Diffusion temp=1000 time=30 dryO2

Diffusion temp=1000 time=30 N2

Diffusion temp=1000 time=90 t.final=400 N2
```

```
$ Field oxide patterning
DEPOSIT PHOTORESIST POSITIVE THICKNESS=1
EXPOSE MASK= Field
DEVELOP
ETCH OXIDE
ETCH PHOTORESIST ALL

$Print layer information
Select Z=doping
Print.1D X.V=0.5 layers
Print.1D X.V=3.0 layers
Print.1D X.V=5.0 layers
$ Save structure
SAVEFILE OUT.FILE=File1_out

$ Plot the initial structure
SELECT Z=LOG10(BORON) TITLE="Patterned Field Oxide"
PLOT.2D SCALE GRID C.GRID=2 Y.MAX=2.0
PLOT.2D SCALE Y.MAX=2.0
$ Color fill the regions
COLOR SILICON COLOR=5
COLOR OXIDE COLOR=7
$ Plot contours of boron
FOREACH X (15 TO 20 STEP 0.5)
CONTOUR VALUE=X LINE=5 COLOR=2
END
```

$ Replot boundaries

PLOT.2D ^AX ^CL

$ Print doping information under field oxide area

SELECT Z=DOPING

PRINT.1D X.VALUE=4.5 X.MAX=2.5

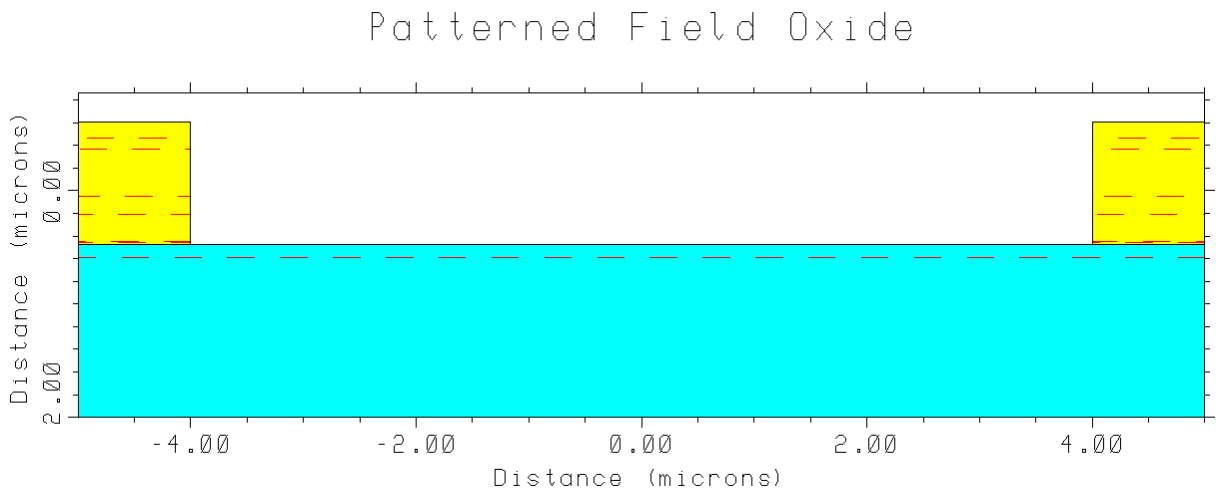

Figure 1.4.1 Cross-section of patterned field oxide from TSUPREM simulations.

1.4.1.3 Gate oxide, Poly Si growth, S/D formation and implantation:

After defining active area, gate oxide was grown of ~100µm through dry oxidation. Then about ~66µm thick polysilicon layer was grown on top of it by sputtering. Then both the oxide layer and polysilicon layer were patterned and source and drain doping was obtained by ion implantation with a dose of 2E15cm^{-2} and energy of 150keV. The cross-section after polysilicon and gate oxide etching as well as after source and drain doping is simulated in this part.

Code for Gate and PolySi deposition, Source/Drain definition and doping:

$Gate ox growth, Poly Deposit & S/D implant

$ Set grid spacing and accuracy parameters

MESH GRID.FAC=1.5

$ Read structure from earlier simulation

```
INITIAL IN.FILE=File1_out
$ Read the mask definition file
MASK IN.FILE=Mask1.tl1

$ Gate oxide growth
Diffusion temp=400 time=90 t.final=1050 N2
Diffusion temp=1050 time=60 N2
Diffusion temp=1050 time=75 dryO2
Diffusion temp=1050 time=30 N2
Diffusion temp=1050 time=90 t.final=400 N2

$ Poly deposition
DEPOSIT POLYSILICON THICKNESS=0.66
PRINT LAYERS X.VALUE=2.5

$ Pattern poly
DEPOSIT PHOTORESIST POSITIVE THICKNESS=1
EXPOSE MASK = Poly
DEVELOP
ETCH POLYSILI
ETCH PHOTORESIST ALL

$ Pattern gate oxide
DEPOSIT PHOTORESIST POSITIVE THICKNESS=1
EXPOSE MASK= Gate
DEVELOP
ETCH OXIDE
```

```
ETCH PHOTORESIST ALL

$ Arsenic implantation for S/D
IMPLANT ARSENIC DOSE=2E15 ENERGY=150 TILT 7

$ Plot structure
SELECT Z=LOG10(BORON) TITLE="S/D Doping by Ion Implantation"
PLOT.2D SCALE Y.MAX=2.0
SELECT Z=LOG10(ARSENIC)
PLOT.1D ^AXES ^CLEAR LINE.TYP=2 COLOR=1


$ Add color fill
COLOR SILICON COLOR=5
COLOR OXIDE COLOR=7
COLOR POLY COLOR=6

$ Plot contours
SELECT Z=LOG10(ARSENIC)
FOREACH X (14 TO 21)
CONTOUR VALUE=X LINE=2 COLOR=4
END

$ Replot boundaries
PLOT.2D ^AX ^CL

$ Save structure
```

SAVEFILE OUT.FILE=File1_out2

SELECT Z=LOG10(BORON) TITLE="Doping Concentrations at Source/Drain" LABEL=LOG(CONCENTRATION)

PLOT.1D X.V=3 BOTTOM=13 TOP=21.5 RIGHT=1 LINE.TYP=4 COLOR=6

SELECT Z=LOG10(ARSENIC)

PLOT.1D X.V=3 ^AXES ^CLEAR LINE.TYP=2 COLOR=1

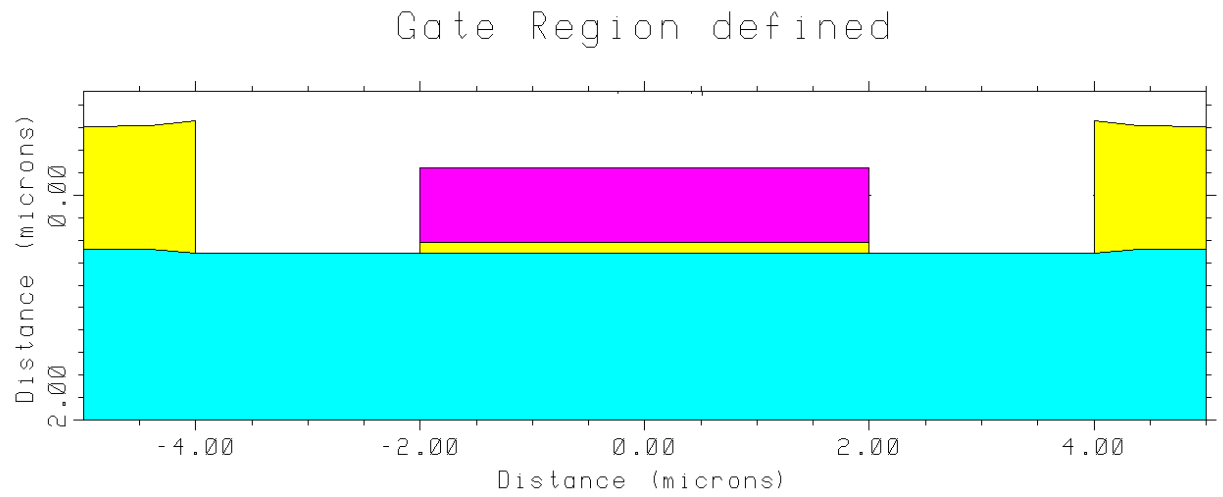

Figure 1.4.2 Cross-section of patterned gate oxide and polysilicon defining source and drain region from TSUPREM simulations.

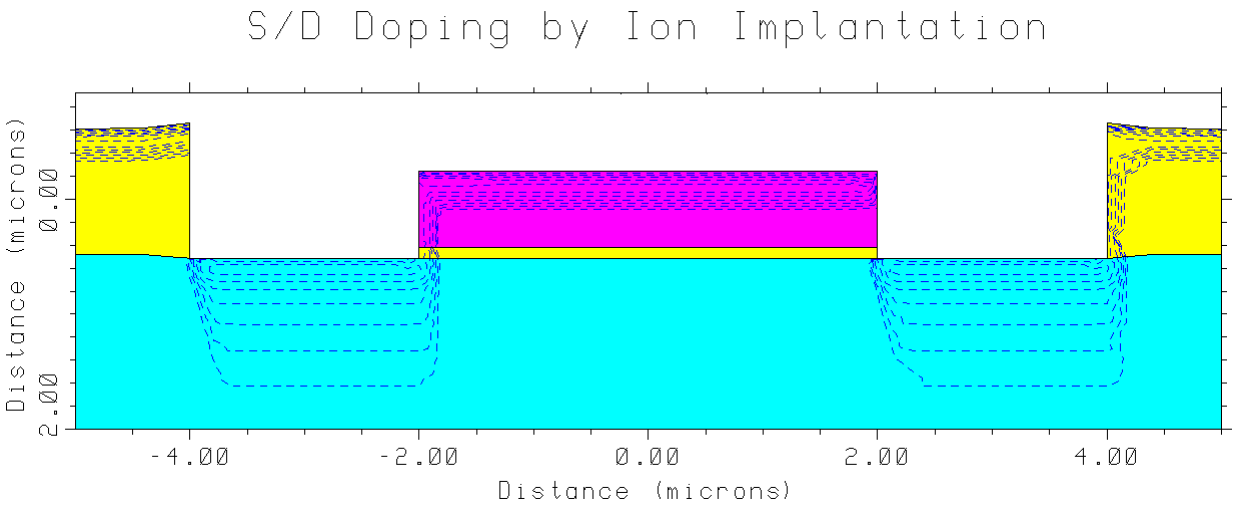

Figure 1.4.3 Cross-section of patterned gate oxide and polysilicon with doped source and drain region from TSUPREM simulations.

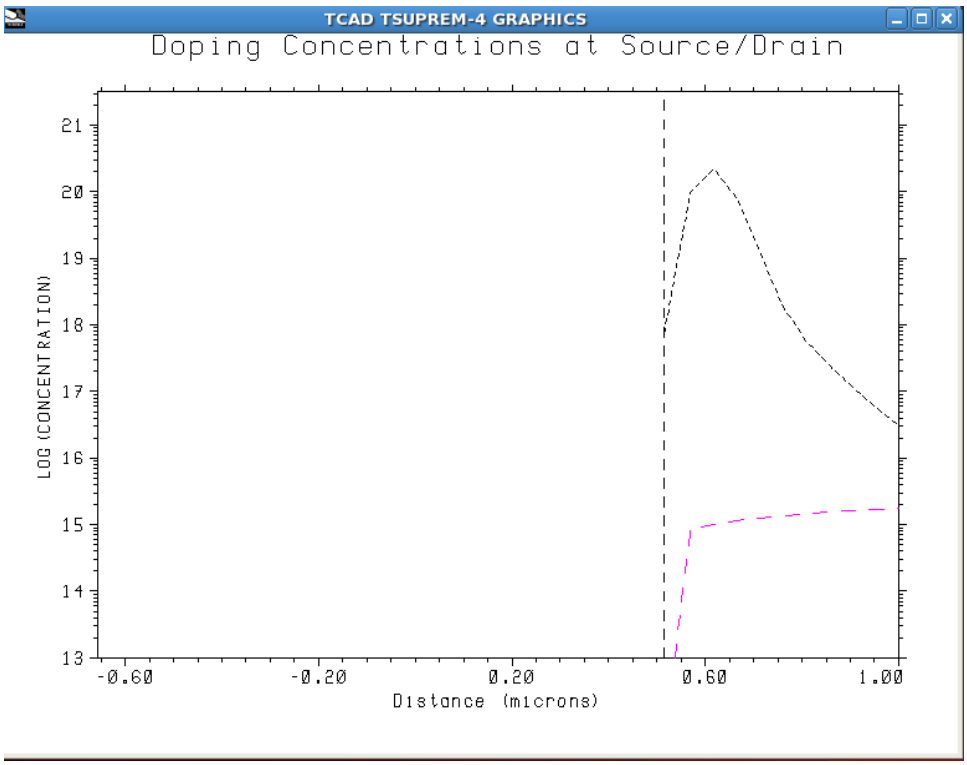

Figure 1.4.4 Doping concentration in source and drain with black dotted line showing log_{10} (As concentration) and red dotted line showing log_{10}(B concentration).

1.4.1.4 ILD and Metal Deposition:

After source and drain implantation, ILD of thickness 800nm was deposited. Then the wafer was annealed to densify the ILD and activate the implant. Then Al was deposited and patterned. The final NMOS structure was completed.

Code for ILD and Metal deposition:

$ ILD Deposit & S/D metallization

$ Set grid spacing and accuracy parameters

MESH GRID.FAC=1.5

$ Read structure from initial simulation

INITIAL IN.FILE=File1_out2

$ Read the mask definition file

MASK IN.FILE=Mask1.tl1

```
$ Deposit ILD and cut source/drain contact holes
DEPOSIT OXIDE THICKNES=0.8

$ Anneal to make dopant active and densify ILD
DIFFUSION TEMP=1000 TIME=20 N2
DIFFUSION TEMP=600 TIME=360 N2

DEPOSIT PHOTORESIST POSITIVE THICKNESS=1.0
EXPOSE MASK=Contact
DEVELOP
ETCH OXIDE
ETCH PHOTORESIST ALL

$ Define the metallization
DEPOSIT ALUMINUM THICKNESS=1.0
DEPOSIT PHOTORESIST POSITIVE THICKNESS=1.0
EXPOSE MASK = Metal
DEVELOP
ETCH ALUMINUM
ETCH PHOTORESIST ALL

$ Save the final structure
SAVEFILE OUT.FILE=File1_out3
$ Plot the full structure
SELECT Z=LOG10(BORON) TITLE="NMOS_Final Structure"
PLOT.2D SCALE Y.MAX=2.0 GRID C.GRID=2
```

```
PLOT.2D SCALE Y.MAX=2.0
$ Color fill
COLOR SILICON COLOR=5
COLOR OXIDE COLOR=7
COLOR POLY COLOR=6
COLOR ALUM COLOR=2

$ Plot contours
FOREACH X (14 TO 20 STEP 0.5)
CONTOUR VALUE=X LINE=5 COLOR=2
END
SELECT Z=LOG10(ARSENIC)
FOREACH X (14 TO 20)
CONTOUR VALUE=X LINE=2 COLOR=4
END
$ Replot boundaries
PLOT.2D ^AX ^CL

$ Print doping in different layers
SELECT Z=DOPING
PRINT.1D X.VALUE=0.5 LAYERS
PRINT.1D X.VALUE=3 LAYERS
PRINT.1D X.VALUE=5 LAYERS

ELECTRODE NAME= Substrate BOTTOM
```

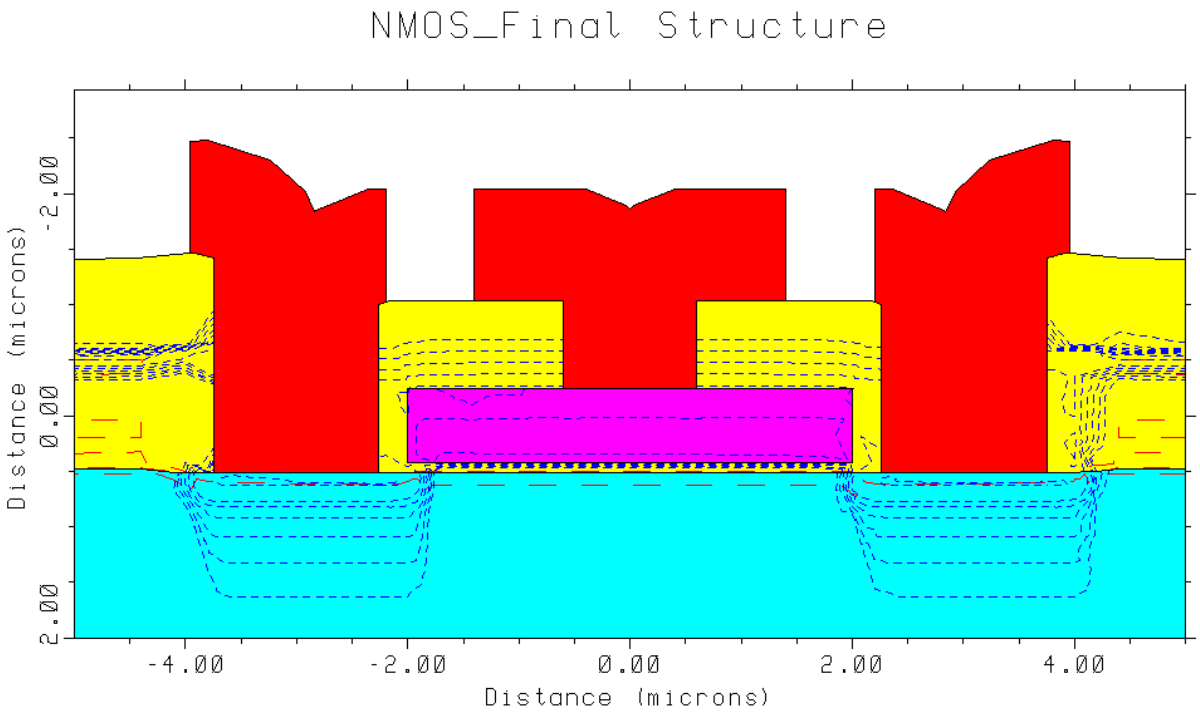

Figure 1.4.5 NMOS final device structure after ILD and metal deposition and patterning with arsenic and boron concentrations with red showing aluminum, yellow showing oxide, pink showing poly and blue showing Si.

```
$ Print doping in different layers
SELECT Z=DOPING
PRINT.1D X.VALUE=0.5 LAYERS

 Num      Material       Top      Bottom  Thickness        Integral
   1      aluminum   -2.0413     -0.2413     1.8000      0.0000e+00
   2   polysilicon   -0.2413      0.4187     0.6600      1.7965e+15
   3         oxide    0.4187      0.5141     0.0954      2.7396e+12
   4         oxide    0.5141      0.5145     0.0005     -6.4312e+07
   5       silicon    0.5145    200.0000   199.4855     -3.9857e+13

PRINT.1D X.VALUE=3 LAYERS

 Num      Material       Top      Bottom  Thickness        Integral
   1      aluminum   -2.0868      0.5146     2.6014      0.0000e+00
   2       silicon    0.5146      1.2583     0.7437      9.4641e+14
   3       silicon    1.2583    200.0000   198.7417     -3.9722e+13

PRINT.1D X.VALUE=5 LAYERS

 Num      Material       Top      Bottom  Thickness        Integral
   1         oxide   -1.4114     -0.3114     1.1000      2.4358e+15
   2         oxide   -0.3114      0.4788     0.7903     -8.4297e+10
   3       silicon    0.4788    200.0000   199.5212     -3.9875e+13
```

From the simulation, the thickness of various layers can be determined. From the above results, in gate region, the thickness of Al is 1.8μm, polysilicon is 660nm and oxide is 95.4nm. In S/D region, thickness of Al is 2.6 μm.

1.4.1.5 Electrical Characterizations:

1.4.1.5.1 Transfer Characteristics (I_{DS}~V_{GS}):

TSUPREM4 was used to simulate the transfer characteristics of the processed NMOSFET with channel length of 4µm. The gate voltage was varied from -1V to 5V and drain voltage was kept constant at V. The threshold voltage from the characteristics was found to be ~0.1V.

Code for the I_{DS}~V_{GS} Characteristics:

```
$ Id-vg CHARACTERISTICS AND THRESHOLD VOLTAGE MEASUREMENT
$ READ COMPLETE STRUCTURE
INITIAL IN.FILE=File1_out3
$ Extract the gate bias vs. the sheet conductance in channel region
ELECTRIC X=0 THRESHOLD NMOS V="-1 5 0.05" OUT.FILE=File1_out4.txt

$ Plot the Vgs vs Ids
$  Define the scale to convert the sheet conductance to the current
ASSIGN NAME=Lch N.VAL=2
ASSIGN NAME=Wch N.VAL=10
ASSIGN NAME=Vds N.VAL=0.1
ASSIGN NAME=Scale N.VAL=(@Vds*@Wch/@Lch)
$ -- Plot
SELECT TITLE="NMOS:Transfer Characteristics (Ids vs. Vgs)"
PLOT.1D IN.FILE=File1_out4.txt Y.SCALE=@Scale +
Y.LABEL="I(Drain) (Amps)" X.LABEL="V(Gate) (Volts)" +
TOP=1.5E-4 BOT=-1E-7 COLOR=2
```

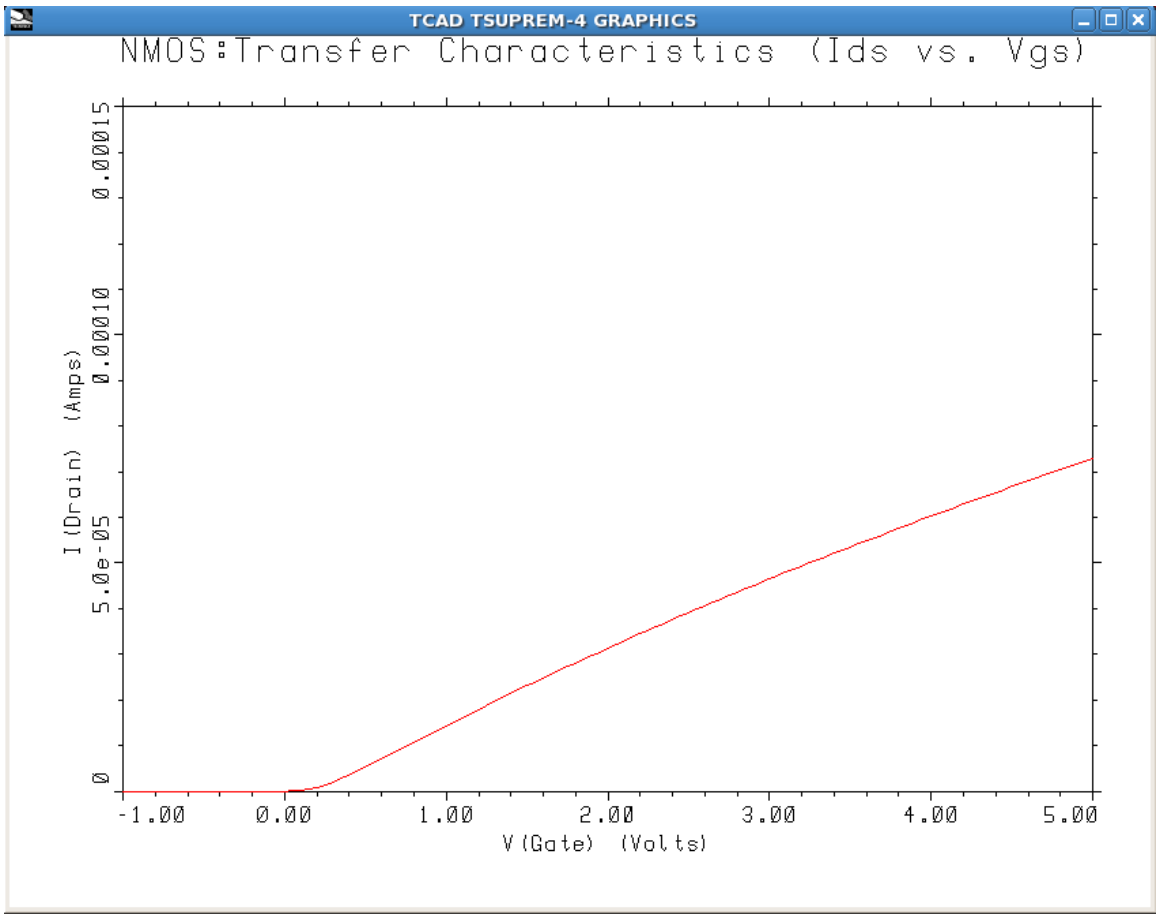

Figure 1.4.6 NMOSFET with L=4μm simulated transfer characteristics with V_{th} =~0.1V.

1.4.1.5.2 C~V Characteristics:

The NMOSFET structure was also simulated for C~V characteristics at both low and high frequency as well as deep depletion. The blue dotted curve shows the low frequency curve, green dotted line shows the high frequency and the red dotted line is for deep depletion. The threshold voltage was found to be same ~0.1V as transfer characteristics.

Code for C~V characteristics:

```
$C-V plot for MOS capacitance

INITIAL IN.FILE=File1_out3

$ -- High Frequency

ELECTRIC X=0.0 MOSCAP NMOS V="-5 5 0.05"  OUT.F=High_Freq.txt


$ -- Low Frequency
```

```
ELECTRIC X=0.0 MOSCAP NMOS V="-5 5 0.05"  LOW OUT.F=Low_Freq.txt
$ -- Deep depletion
ELECTRIC X=0.0 MOSCAP NMOS V="-5 5 0.05"  DEEP OUT.F=Deep.txt
SELECT TITLE="NMOS: C-V Characteristics"
PLOT.1D ELECTRIC COLOR=2 TOP=7E-8 BOT=0 LEFT=-6 RIGHT=6  ^CL
PLOT.1D IN.FILE=High_Freq.txt ^CL ^AX COLOR=3 LINE=2
PLOT.1D IN.FILE=Low_Freq.txt ^CL ^AX COLOR=4 LINE=3
```

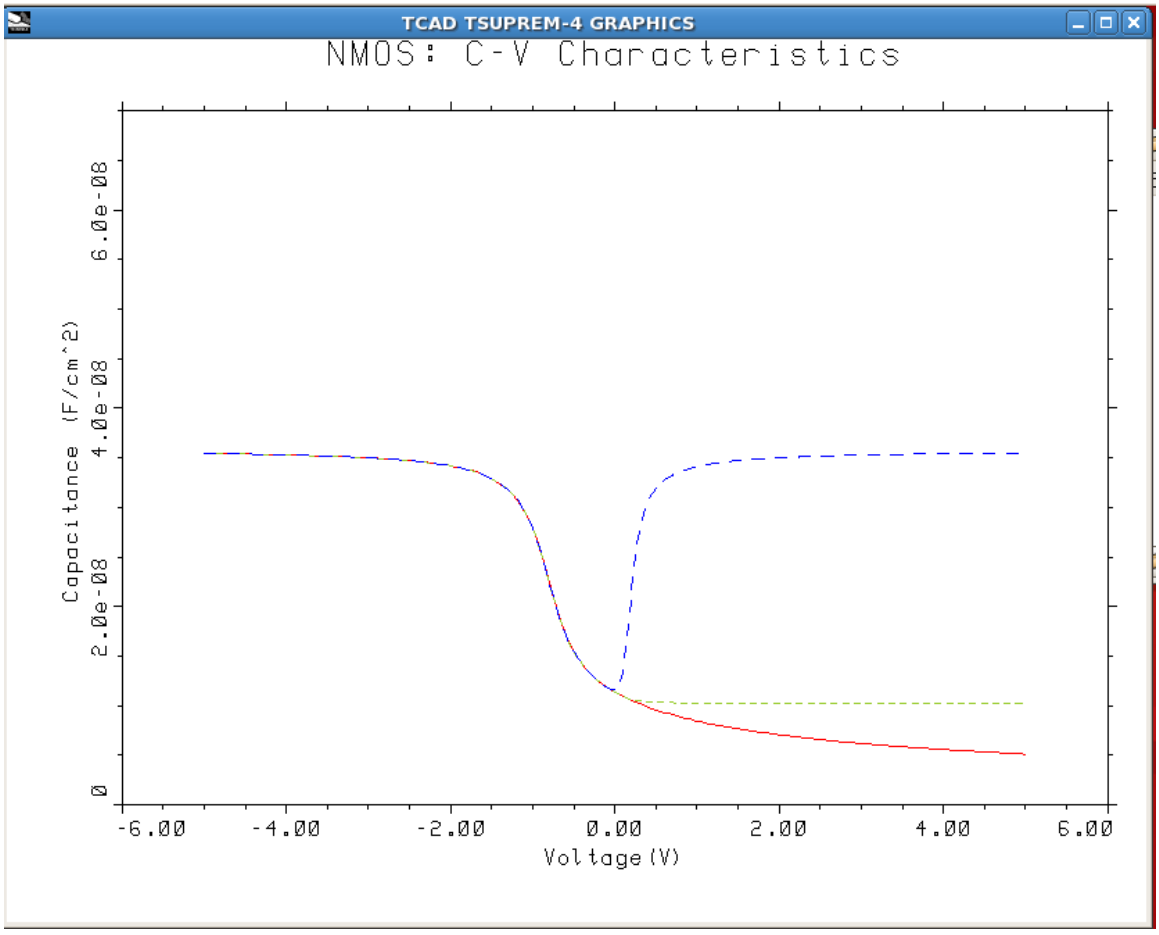

Figure 1.4.7 NMOSFET with L=4μm simulated C~V characteristics in low, high frequencies as well as deep depletion.

1.4.2 PMOS Process Simulation:

Similar to NMOS processing PMOS processing also goes through similar steps on an n-type <100> phosphorous doped Si substrate, but with the exception of doping with BORON with lower energy and additional Si_3N_4 layer to prevent the boron diffusion.

1.4.2.1 Mask Definition:

PMOS mask was defined for a channel length of 4µm and scaling factor of 1000. Mask for PMOS similar to NMOS contains 5 masks, such as: Field, Gate, Poly, Contact and Metal.

Code:

TL1 0100

/Channel length =4um

/Scaling factor = 1000

/

1000

-5000 5000

5

Field 2

-5000 -4000

4000 5000

Gate 3

-5000 -4000

-2000 2000

4000 5000

Poly 1

-2000 2000

Contact 4

-5000 -3750

-2260 -600

600 2260

3750 5000

Metal 3

-3960 -2200

-1400 1400

2200 3960

1.4.2.2 Field Oxide Growth and Patterning:

Field oxide of a thickness of 1 µm was grown on top of the n-type Si substrate and then it was patterned using lithography to expose a region of 8 µm in the center. This region is known as the active area of the device. For field oxide growth a combination of dry and wet oxidation steps were followed. The TSUPREM4 code for the program is given below along with the patterned field oxide cross-section.

Code for Field oxide growth and patterning:

$Field oxidation and patterning for PMOS

$ Define the grid

MESH GRID.FAC=1.5

$ Read the mask definition file

$MASK IN.FILE=Mask1.tl1 PRINT GRID="Field,Poly"

MASK IN.FILE=Mask1.tl1 PRINT GRID="Field,Poly"

$ p-type substrate initialization

INITIALIZE <100> PHOSPHOR=2E15 I.RESIST=10

$Field oxide growth

Diffusion temp=400 time=90 t.final=1000 N2

Diffusion temp=1000 time=60 N2

```
Diffusion temp=1000 time=30 dryO2
Diffusion temp=1000 time=300 wetO2
Diffusion temp=1000 time=30 dryO2
Diffusion temp=1000 time=30 N2
Diffusion temp=1000 time=90 t.final=400 N2

$ Field oxide patterning
DEPOSIT PHOTORESIST POSITIVE THICKNESS=1
EXPOSE MASK= Field
DEVELOP
ETCH OXIDE
ETCH PHOTORESIST ALL

$Print layer information
Select Z=doping
Print.1D X.V=0.5 layers
Print.1D X.V=3.0 layers
Print.1D X.V=5.0 layers
$ Save structure
SAVEFILE OUT.FILE=File1_out

$ Plot the initial structure
SELECT Z=LOG10(PHOSPHOR) TITLE="Patterned Field Oxide"
PLOT.2D SCALE GRID C.GRID=2 Y.MAX=2.0
PLOT.2D SCALE Y.MAX=2.0
$ Color fill the regions
COLOR SILICON COLOR=5
```

```
COLOR OXIDE COLOR=7
$ Plot contours of phosphorous
FOREACH X (15 TO 20 STEP 0.5)
CONTOUR VALUE=X LINE=5 COLOR=2
END
$ Replot boundaries
PLOT.2D ^AX ^CL
$ Print doping information under field oxide area
SELECT Z=DOPING
PRINT.1D X.VALUE=4.5 X.MAX=2.5
```

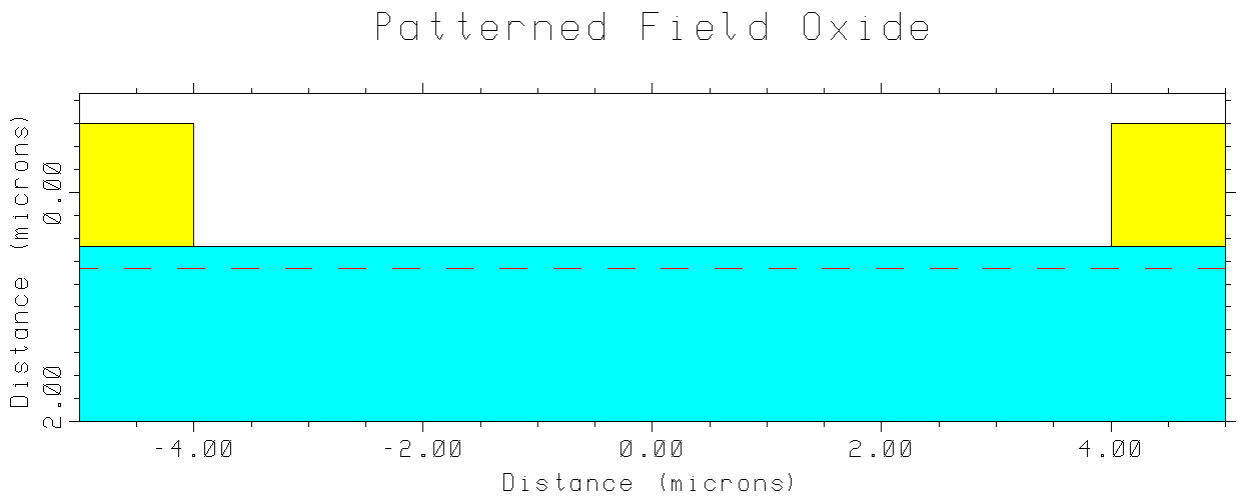

Figure 1.4.8 Cross-section of patterned gate oxide and polysilicon defining source and drain region from TSUPREM simulations.

1.4.2.3 Gate oxide, Poly Si growth, S/D formation and implantation:

After defining active area, gate oxide was grown of ~100µm through dry oxidation. Then about ~66µm thick polysilicon layer was grown on top of it by sputtering. Then both the oxide layer and polysilicon layer were patterned and source and drain doping was obtained by ion implantation of Boron with a dose of 2E15cm^{-2} and energy of 50keV. The cross-section after polysilicon and gate oxide etching as well as after source and drain doping is simulated in this part.

Code for Gate and PolySi deposition, Source/Drain definition and doping:

```
$Gate oxide growth, Poly Deposit & S/D implant for PMOS
$ Set grid spacing and accuracy parameters
MESH GRID.FAC=1.5
$ Read structure from earlier simulation
INITIAL IN.FILE=File1_out
$ Read the mask definition file
MASK IN.FILE=Mask1.tl1

$ Gate oxide growth
Diffusion temp=400 time=90 t.final=1050 N2
Diffusion temp=1050 time=60 N2
Diffusion temp=1050 time=75 dryO2
Diffusion temp=1050 time=30 N2
Diffusion temp=1050 time=90 t.final=400 N2

$ Poly deposition
DEPOSIT POLYSILICON THICKNESS=0.66
PRINT LAYERS X.VALUE=2.5

$ Pattern poly
DEPOSIT PHOTORESIST POSITIVE THICKNESS=1
EXPOSE MASK = Poly
DEVELOP
ETCH POLYSILI
ETCH PHOTORESIST ALL
```

```
$ Pattern gate oxide
DEPOSIT PHOTORESIST POSITIVE THICKNESS=1
EXPOSE MASK= Gate
DEVELOP
ETCH OXIDE
ETCH PHOTORESIST ALL

$ BORON implantation for S/D
IMPLANT BORON DOSE=2E15 ENERGY=50 TILT=7

$ Plot structure
SELECT Z=LOG10(BORON) TITLE="Gate region defined and S/D Ion Implantation"
PLOT.2D SCALE Y.MAX=2.0
FOREACH X (15 TO 18)
CONTOUR VALUE=X LINE=5 COLOR=2
END

$ Add color fill
COLOR SILICON COLOR=5
COLOR OXIDE COLOR=7
COLOR POLY COLOR=6

$ Plot contours
SELECT Z=LOG10(BORON)
FOREACH X (16 TO 20)
CONTOUR VALUE=X LINE=2 COLOR=4
END
```

$ Replot boundaries

PLOT.2D ^AX ^CL

$ Save structure

SAVEFILE OUT.FILE=File1_out2

SELECT Z=LOG10(PHOSPHOR) TITLE="Doping Concentrations at Source/Drain" LABEL=LOG(CONCENTRATION)

PLOT.1D X.V=3 BOTTOM=13 TOP=21.5 RIGHT=1 LINE.TYP=4 COLOR=6

SELECT Z=LOG10(BORON)

PLOT.1D X.V=3 ^AXES ^CLEAR LINE.TYP=2 COLOR=1

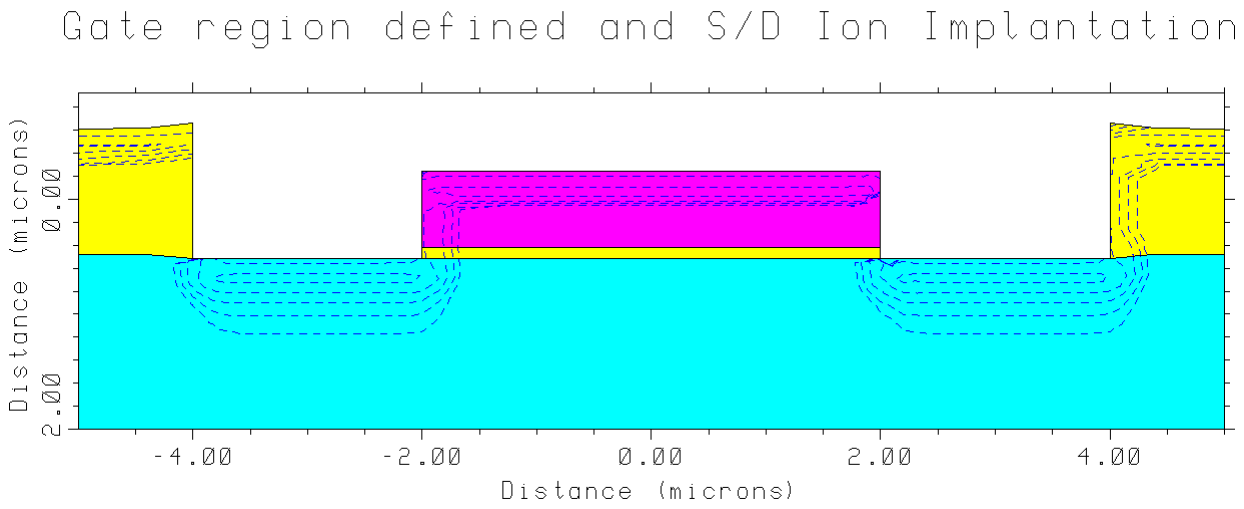

Figure 1.4.9 Cross-section of patterned gate oxide and polysilicon with boron doped source and drain region from TSUPREM simulations.

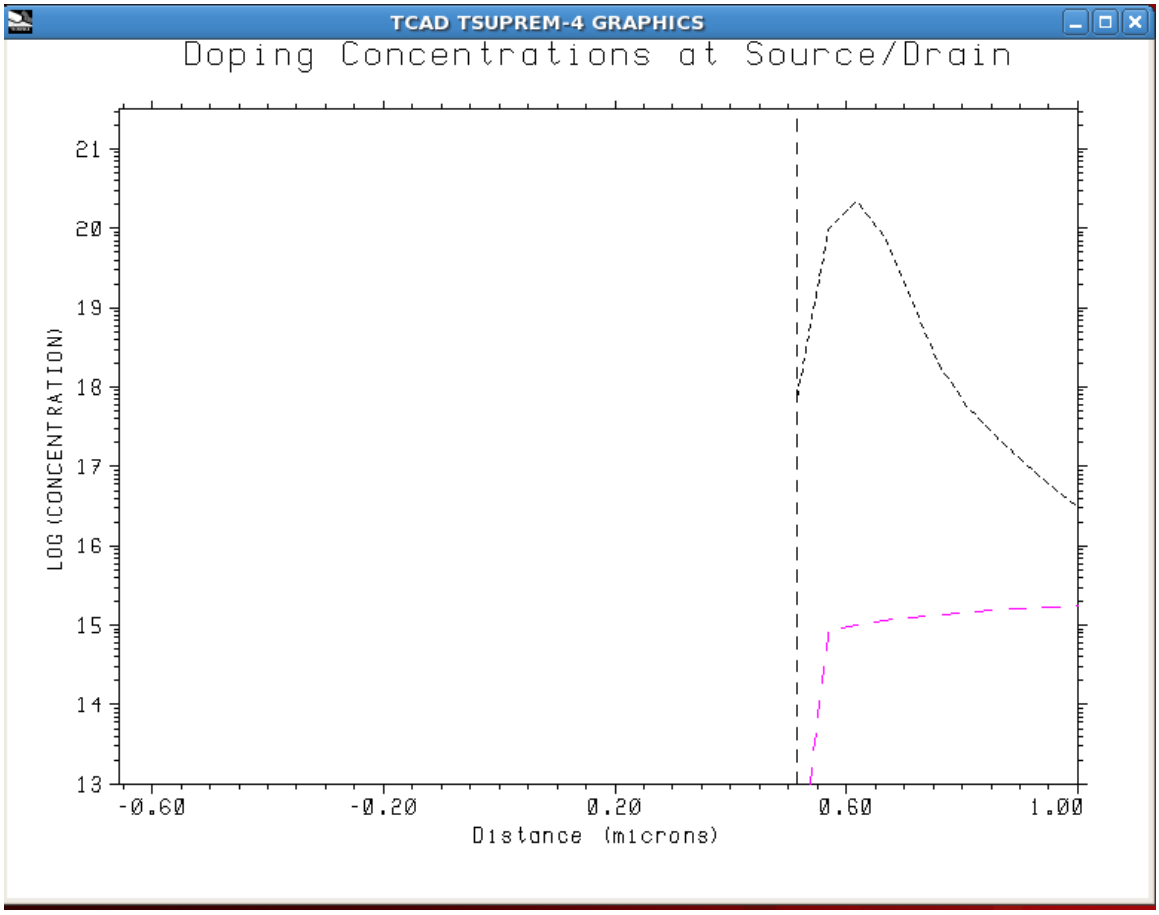

Figure 1.4.10 Doping concentration in source and drain with black dotted line showing log_{10} (B concentration) and red dotted line showing log_{10}(Phosphorous concentration).

1.4.2.4 ILD and Metal Deposition:

After source and drain implantation, ILD of thickness 700nm with Si_3N_4 of thickness 100nm was deposited. Then the wafer was annealed to densify the ILD and activate the implant. Nitride layer and ILD were etched. Then Al was deposited and patterned. The final NMOS structure was completed.

Code for ILD and Metal deposition:

$ ILD Deposit & S/D metallization for PMOS

$ Set grid spacing and accuracy parameters

MESH GRID.FAC=1.5

$ Read structure from initial simulation

```
INITIAL IN.FILE=File1_out2
$ Read the mask definition file
MASK IN.FILE=Mask1.tl1

$ Deposit ILD and cut source/drain contact holes
DEPOSIT NITRIDE THICKNES=0.1
DEPOSIT OXIDE THICKNES=0.7

$ Anneal to make dopant active and densify ILD
DIFFUSION TEMP=1000 TIME=20 N2
DIFFUSION TEMP=600 TIME=360 N2

DEPOSIT PHOTORESIST POSITIVE THICKNESS=1.0
EXPOSE MASK=Contact
DEVELOP
ETCH OXIDE
ETCH NITRIDE
ETCH PHOTORESIST ALL

$ Define the metallization
DEPOSIT ALUMINUM THICKNESS=1.0
DEPOSIT PHOTORESIST POSITIVE THICKNESS=1.0
EXPOSE MASK = Metal
DEVELOP
ETCH ALUMINUM
ETCH PHOTORESIST ALL
```

```
$ Save the final structure
SAVEFILE OUT.FILE=File1_out3
$ Plot the full structure
SELECT Z=LOG10(BORON) TITLE="PMOS_Final Structure"
PLOT.2D SCALE Y.MAX=2.0 GRID C.GRID=2
PLOT.2D SCALE Y.MAX=2.0
$ Color fill
COLOR SILICON COLOR=5
COLOR OXIDE COLOR=7
COLOR POLY COLOR=6
COLOR ALUM COLOR=2
COLOR NITRIDE COLOR=3

$ Plot contours
FOREACH X (15 TO 18 STEP 0.5)
CONTOUR VALUE=X LINE=5 COLOR=2
END
SELECT Z=LOG10(BORON)
FOREACH X (14 TO 20)
CONTOUR VALUE=X LINE=2 COLOR=4
END
$ Replot boundaries
PLOT.2D ^AX ^CL

$ Print doping in different layers
SELECT Z=DOPING
PRINT.1D X.VALUE=0.5 LAYERS
```

PRINT.1D X.VALUE=3 LAYERS

PRINT.1D X.VALUE=5 LAYERS

ELECTRODE NAME= Substrate BOTTOM

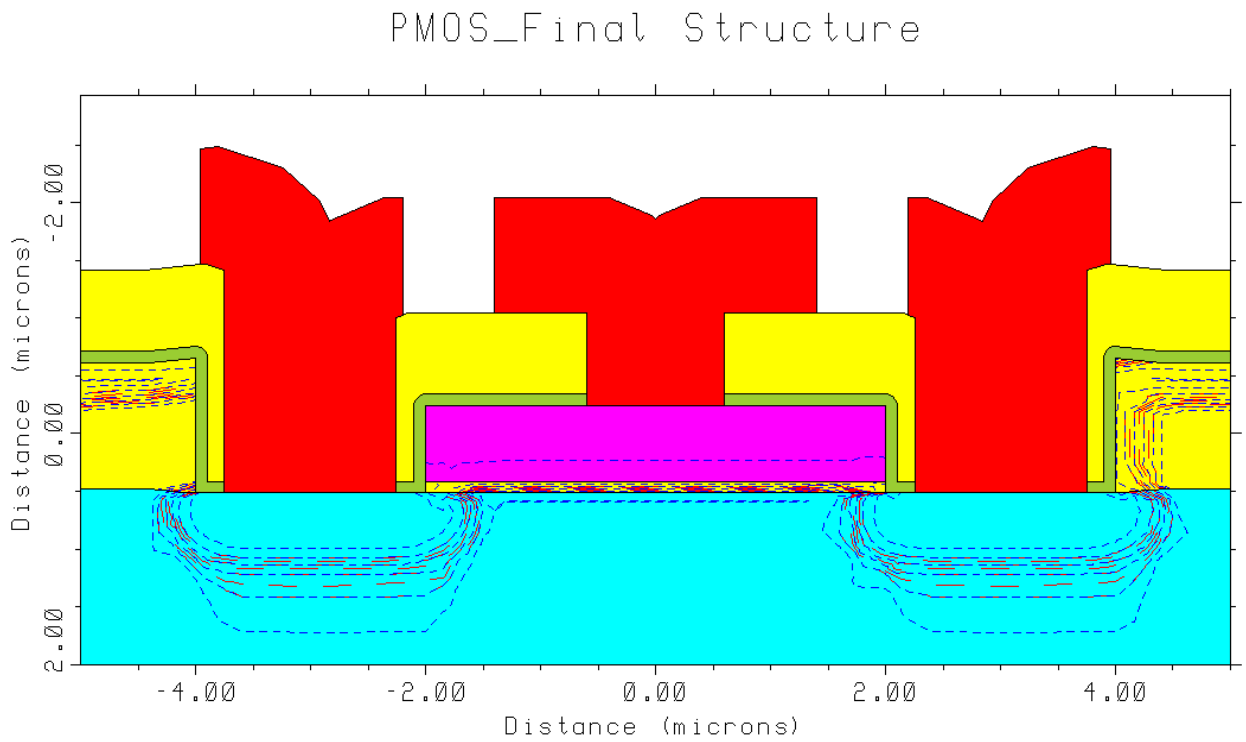

Figure 1.4.11 PMOS final device structure after ILD and metal deposition and patterning with boron and phosphor concentrations, green layer showing nitride, red showing aluminum, yellow showing oxide, pink showing poly and blue showing Si.

```
$ Print doping in different layers
SELECT Z=DOPING
PRINT.1D X.VALUE=0.5 LAYERS

 Num      Material       Top     Bottom  Thickness        Integral
   1      aluminum   -2.0416    -0.2416     1.8000      0.0000e+00
   2   polysilicon   -0.2416     0.4184     0.6600     -8.6144e+14
   3         oxide    0.4184     0.5143     0.0958     -3.3883e+14
   4       silicon    0.5143   200.0000   199.4857      3.9963e+13

PRINT.1D X.VALUE=3 LAYERS

 Num      Material       Top     Bottom  Thickness        Integral
   1      aluminum   -2.0864     0.5143     2.6006      0.0000e+00
   2       silicon    0.5143     1.3585     0.8443     -8.4853e+14
   3       silicon    1.3585   200.0000   198.6415      3.9705e+13

PRINT.1D X.VALUE=5 LAYERS

 Num      Material       Top     Bottom  Thickness        Integral
   1         oxide   -1.4111    -0.7111     0.7000      0.0000e+00
   2       nitride   -0.7111    -0.6111     0.1000      0.0000e+00
   3         oxide   -0.6111    -0.1612     0.4498     -1.8292e+15
   4         oxide   -0.1612     0.4785     0.6398      2.0825e+10
   5       silicon    0.4785   200.0000   199.5215      3.9966e+13
```

Thickness of various layers is as shown in the above figure.

1.4.2.5 Electrical Characterizations

1.4.2.5.1 Transfer Characteristics (I_{DS}~V_{GS}):

TSUPREM4 was used to simulate the transfer characteristics of the processed PMOSFET with channel length of 4µm. The gate voltage was varied from -5V to 1V and drain voltage was kept constant at V. The threshold voltage from the characteristics was found to be ~ -0.5V.

Code for the I_{DS}~V_{GS} Characteristics:

```
$ Id-vg characteristics and threshold voltage measurement for PMOS

$ Read complete structure

INITIAL IN.FILE=File1_out3

$ Extract the gate bias vs. the sheet conductance in channel region

ELECTRIC X=0 THRESHOLD PMOS V="-5 1 0.05" OUT.FILE=File1_out4.txt


$ Plot the Vgs vs Ids

$ -- Define the scale to convert the sheet conductance to the current

ASSIGN NAME=Lch N.VAL=2

ASSIGN NAME=Wch N.VAL=10

ASSIGN NAME=Vds N.VAL=0.1

ASSIGN NAME=Scale N.VAL=(@Vds*@Wch/@Lch)

$  Plot transfer char

SELECT TITLE="PMOS:Transfer Characteristics (Ids vs. Vgs)"

PLOT.1D IN.FILE=File1_out4.txt Y.SCALE=@Scale +

Y.LABEL="I(Drain) (Amps)" X.LABEL="V(Gate) (Volts)" +

TOP=2E-5 BOT=-1E-7 COLOR=2
```

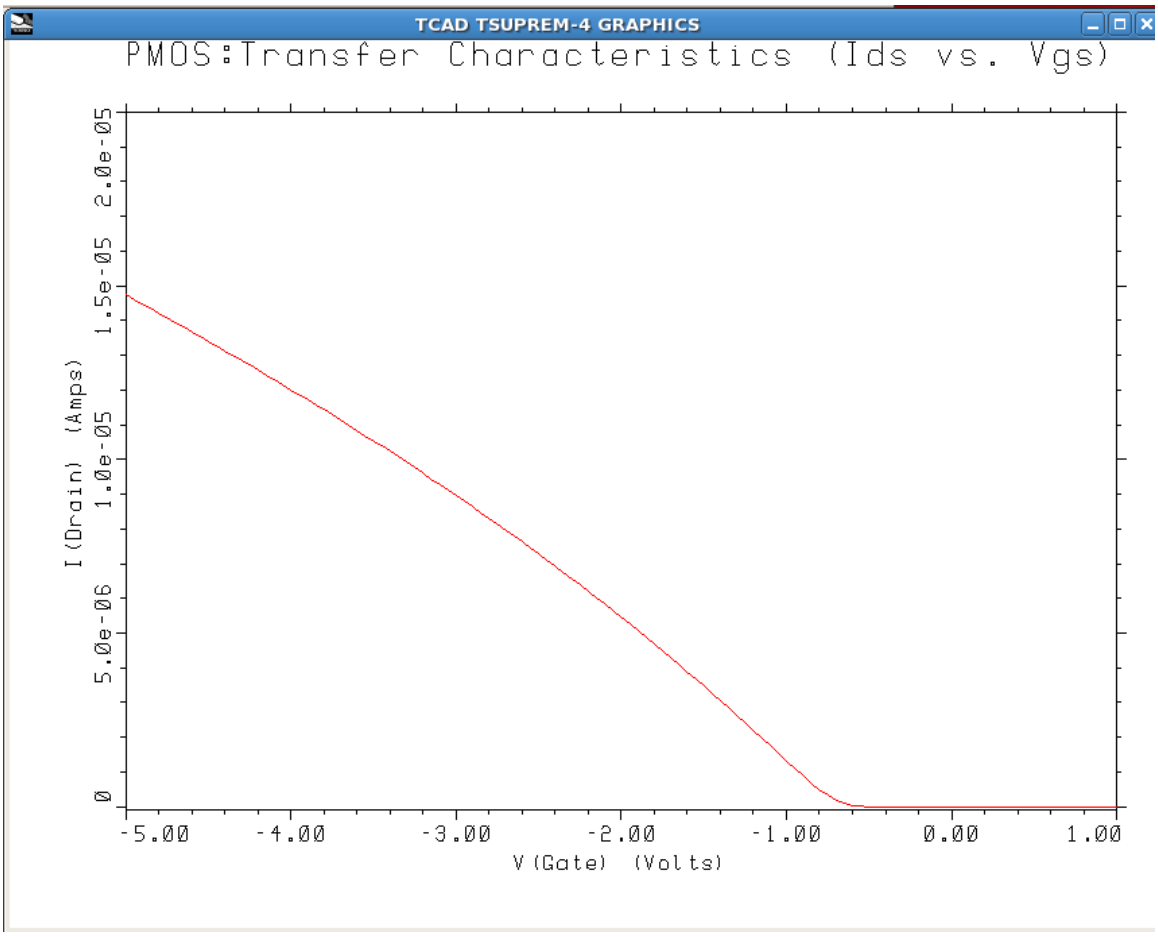

Figure 1.4.12 PMOSFET with L=4µm simulated transfer characteristics with V_{th} =~ -0.5V.

1.4.2.5.2 C~V Characteristics:

The PMOSFET structure was also simulated for C~V characteristics at both low and high frequency as well as deep depletion. The blue dotted curve shows the low frequency curve, green dotted line shows the high frequency and the red dotted line is for deep depletion. The threshold voltage was found to be same ~ -0.5V as transfer characteristics.

Code for C~V characteristics:

```
$C-V plot for PMOS capacitance

INITIAL IN.FILE=File1_out3

$ -- High Frequency

ELECTRIC X=0.0 MOSCAP PMOS V="-5 5 0.05"  OUT.F=High_Freq.txt

$ -- Low Frequency

ELECTRIC X=0.0 MOSCAP PMOS V="-5 5 0.05"  LOW OUT.F=Low_Freq.txt
```

$ -- Deep depletion

ELECTRIC X=0.0 MOSCAP PMOS V="-5 5 0.05" DEEP OUT.F=Deep.txt

SELECT TITLE="PMOS: C-V Characteristics"

PLOT.1D ELECTRIC COLOR=2 TOP=7E-8 BOT=0 LEFT=-6 RIGHT=6 ^CL

PLOT.1D IN.FILE=High_Freq.txt ^CL ^AX COLOR=3 LINE=2

PLOT.1D IN.FILE=Low_Freq.txt ^CL ^AX COLOR=4 LINE=3

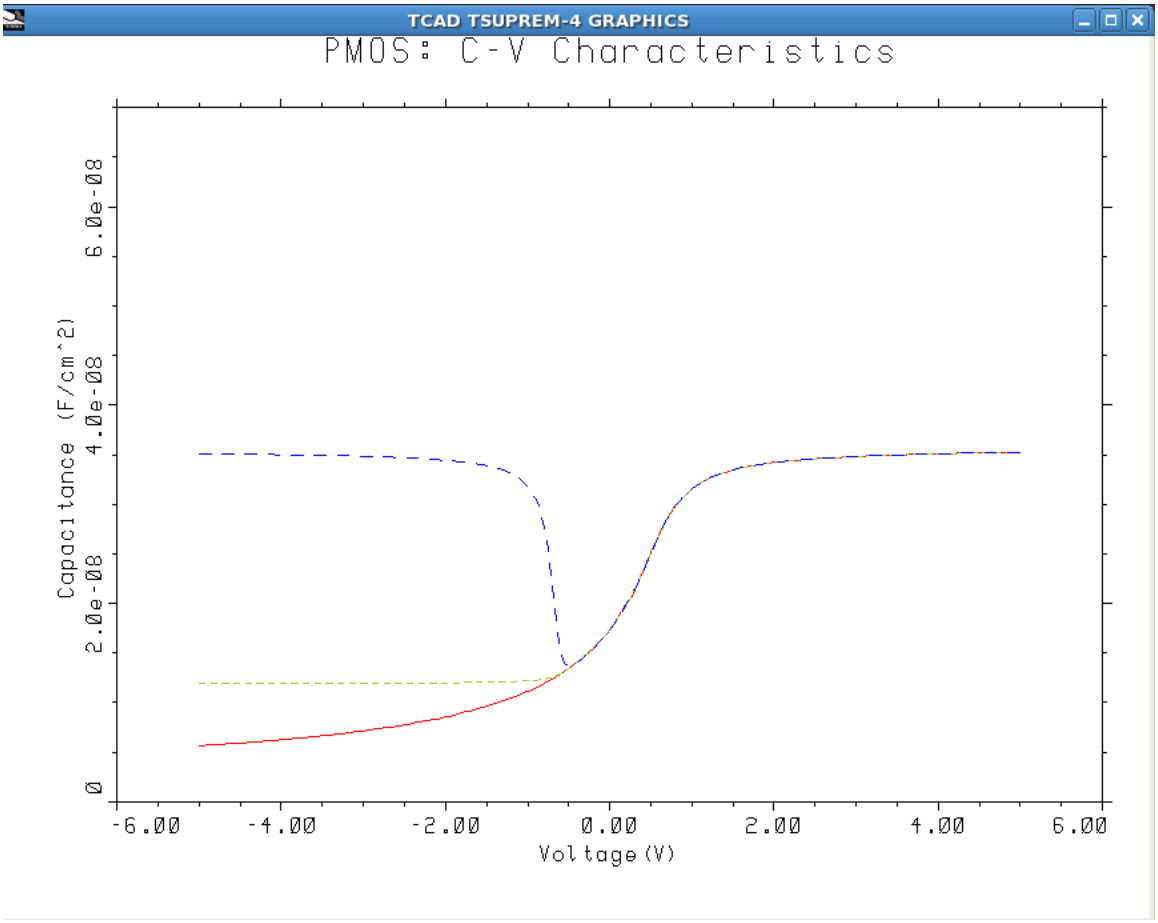

Figure 1.4.13 PMOSFET with L=4μm simulated C~V characteristics in low, high frequencies as well as deep depletion.

1.5 Characterization and Testing

1.5.1 Electrical Contact Measurements

Electrical contact measurements are done to determine the electrical contact resistivity between 2 materials in physical contact. In MOSFET fabrication the contact resistivity we care about is the one between the metal structures and semiconductor. There are different methods of extracting contact resistance and sheet resistance

1.5.1.1 Transmission Line Method:

The transmission line method (TLM) can be used to extract contact resistance and sheet resistance. The transmission line structure is a series of metal contacts of the same area, separated by increasingly higher dimensions. The spacing is linear and 2 probes are assigned to pairs of contacts, and the resistance between them is determined by a applying a voltage sweep and measuring the resulting current. The current flow occurs across the sheet of the semiconductor, through the metal –Semiconductor junction and that is why we can be able to determine sheet resistance and contact resistance

The plot of spacing vs resistance should be close to linear, and a linear regression fit can be used to determine the sheet resistance and contact resistance. The sheet resistance is the slop of the line, while the intercept on the y-axis is two times the contact resistance.

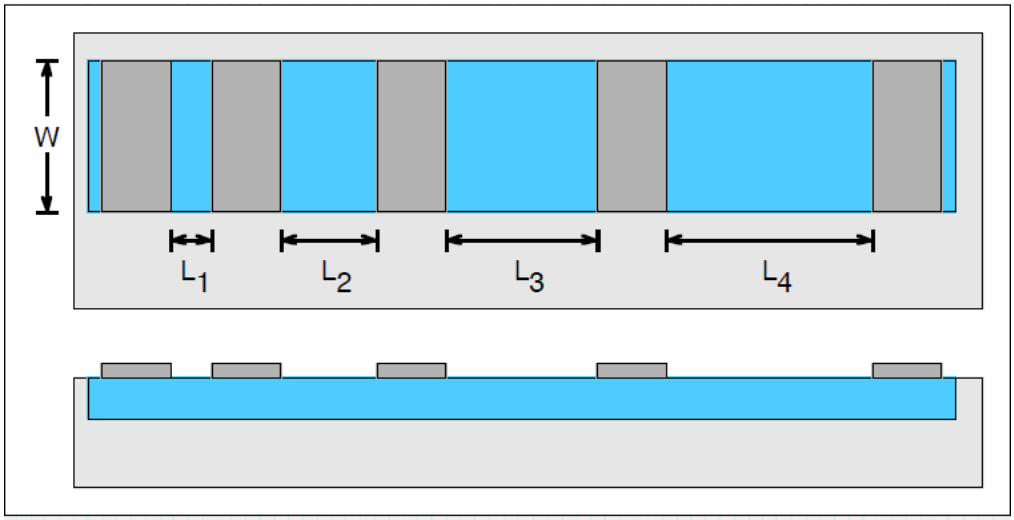

Figure 1.5.1 TLM set-up for determining contact and sheet resistance

For a simple semiconductor with two contacts, the resistance can be measured by

$$Rsemi = Rs\ {}^{L}/_{W};$$

$$Rt = {}^{Rs}/_{W} * L + 2Rc$$

It is using this knowledge that we are able to determine the sheet and contact resistance from the graph as thus:

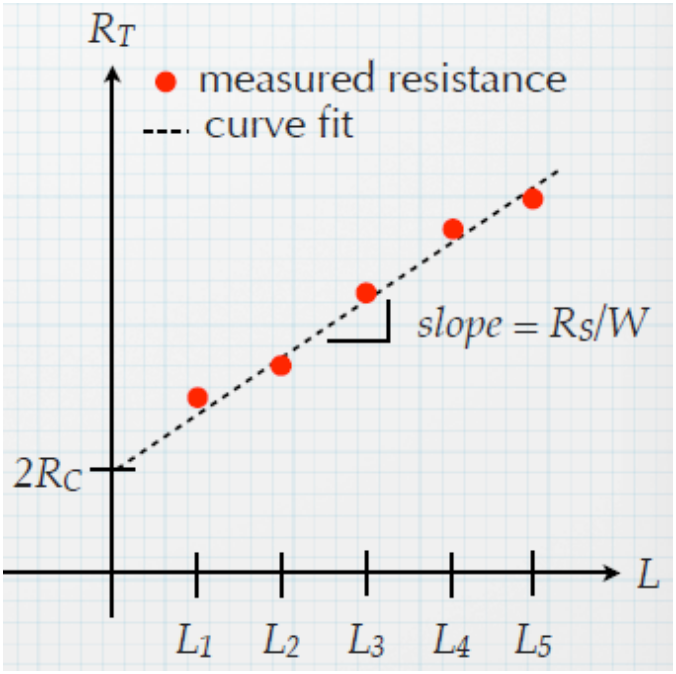

Figure 1.5.2 TLM for estimating Rc and Rs

We can also determine LT, which is the transfer length,

$$L_T = \sqrt{\frac{\rho C}{Rs}}$$

This is the average distance that an electron (or hole) travels in the semiconductor beneath the contacts before it flows up into the contact. The dimensions of the contacts are also a factor in determining contact resistivity, because the flow of electrons into the contact I not uniform and this can also affect t the values that we get because current crowding can occur, this phenomenon would be ignored however because of the small geometry of our contact pads.

1.5.1.2 Kelvin Structure Method:

This is a 4- probe structure that is used to determine contact resistance. Unlike the transmission line where the resistance can be determined traditionally like is done with an ohmmeter. An ammeter is further included that measures the amount of current passing through the semiconductor-metal junction. The two materials to be measured are overlaid on top of each other and current and voltage are measured across materials i.e. for the voltage measurement, one of the probes is on the first material and the other on the second material. The same is done for the current measurements as can be seen in Fig. xx below:

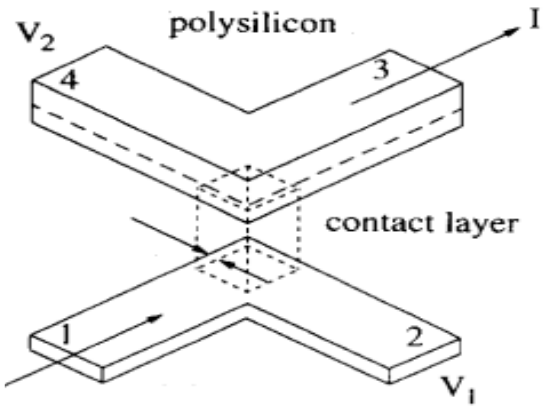

Figure 1.5.3 Kelvin structure for measuring contact resistivity

$R_C = V_{2-4} I_{1-3}$

R_C - Contact resistance

V_{2-4} - Voltage mesured

I_{1-3} - Current forced

$\rho_C = A \times Rc$

A - Area of pad diameter

Rc - Contact resistance

ρ_C - Electrical contact resistivity

The following parameters can then be extracted from the data that we get and this gives us the contact resistance of that pad. The dimensions of the contact can also affect the value of resistance we get, and the actual electrical contact resistivity can be normalized by multiplying contact resistance by the area of the pad.

1.5.2 Sheet Resistance Measurement: Van der Pauw (VdP) Method

This is another structure that can help determine the sheet resistance of thin films. It is a 4 point probe that works in a similar way to the kelvins structure measurements described above. The obvious advantage of the VdP measurement is that it can be used to measure the sheet resistance of films of any shape as long as there are 4 contacts present. The locations of the probes are also important because the probes must be on the boundary or as close as possible as the structure allows.

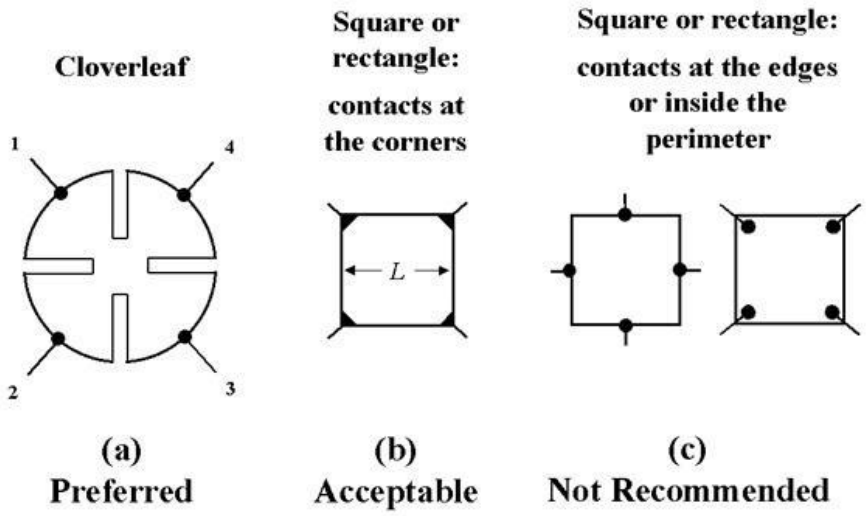

Figure 1.5.4 Probe arrangement for VdP measurements

The ohmic contacts also have to be small as possible because these affect the sheet resistance measured due to the presence of contact resistance. After the measurement the formula for determining the sheet resistance is presented below:

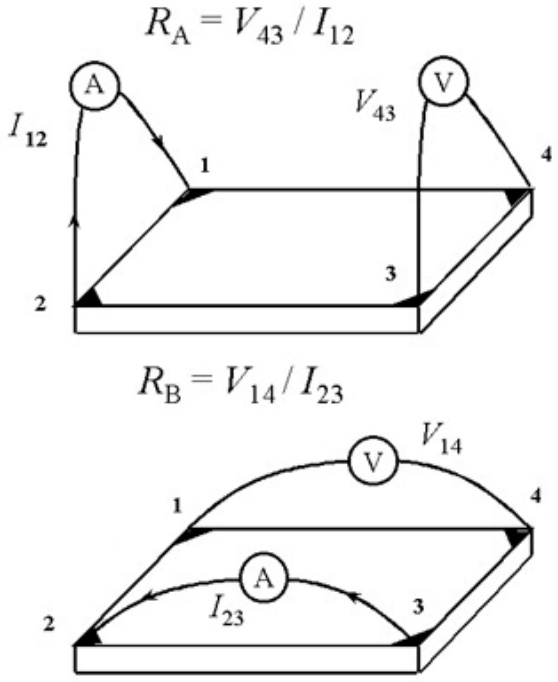

Figure 1.5.5 Voltmeter and Ammeter placement

$e^{-\pi R_{12,34} R_S} + e^{-\pi R_{23,41} R_S} = 1$

$R_{12,341}$ - Total resistance measured

R_S - Sheet resistance
$R_{12,34} = V_{34} I_{12}$ $R_{23,41} = V_{41} I_{23}$
For symmetric structure, like in this report, there is-
$R_{12,34} = R_{23,41}$
$R_S = \pi ln2 \times V_{41} I_{23}$.

1.5.3 C-V Measurements

Capacitance-Voltage measurements, or CV measurements, are taken on MOS capacitor devices, separate from the MOSFETs. A voltage is applied between the metal layer and back contact of the IC. The applied voltage is swept across a range from negative voltage to positive voltage, providing data on the capacitance of the device as a function of the voltage signal. The total capacitance of the device depends on the capacitance of the oxide, the capacitance of the depletion region in the substrate, and the capacitance due to inversion charge below the gate oxide. The capacitance due to inversion charge is sensitive to the AC frequency of the voltage signal, causing the capacitance curve to vary with source frequency.

There are four characteristic features to the CV curve of a MOS device.

Accumulation: Applying a negative voltage to an n-channel MOS capacitor causes the majority carriers in the p-type substrate to segregate at a semiconductor and metal interface. This causes the device to behave like a single parallel plate capacitor with the oxide as a dielectric between the plates. In this case the capacitance is the oxide capacitance, or C_{ox}.

Flatband: As the voltage is increased it reaches a point where the applied voltage causes the energy band of the semiconductor to become flat. This voltage is called the flatband voltage, V_{FB}. The flat band voltage is equal to the difference in the work function between the metal interface and the semiconductor.

Depletion: When the applied voltage begins to exceed V_{FB} the device is in the depletion region. The applied voltage causes the majority carriers to be depleted from the metal-semiconductor interface. In this region the total capacitance can be modeled as two capacitors in series, the

oxide capacitance and the capacitance of the depletion region. The width of the depletion region, and its capacitance, eventually stop increasing as voltage increases. The voltage at which this occurs is the threshold voltage, V_T, and the capacitance of the depletion region at this point is the depletion capacitance.

Inversion: As the applied voltage increases past the threshold voltage an inversion layer of minority carriers forms at the metal-semiconductor interface. If the applied voltage is a low frequency the rate of change of the applied signal is less than the response rate of the minority carriers. In this low frequency case the system again behaves like a parallel plate capacitor and the total capacitance is C_{ox}. At higher frequency applied signals the rate of change in the signal exceeds the response rate of the minority carriers. In this case the system continues to behave as though it is two capacitors in series, the oxide capacitance and the depletion capacitance.

1.5.4 I-V Characteristics

One of the important electrical characteristics of MOSFETs is their current-voltage, or I-V, characteristics. The I_{DS}-V_{DS} characteristics of an ideal MOSFET is shown in Figure 1.5.1. Here, the source-drain current (I_{DS}) is measured as function of source-drain voltage (V_{DS}), and the threshold voltage can be determined from the curves. At a given gate voltage (V_{GS}), the I-V curve shows three different regions: linear, non-linear, and saturation. In the linear region, the drain voltage is much smaller than the overdrive voltage ($V_{DS} \ll V_{GS} - V_{th}$), and the drain current is proportional to the drain voltage, behaving like a resistor. The drain current I_D can be expressed as

$$I_D = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS}$$

where μ is the carrier mobility in the channel, C_{ox} is the oxide capacitance, W is the width of the channel, L is the length of the channel, V_T is the threshold voltage.

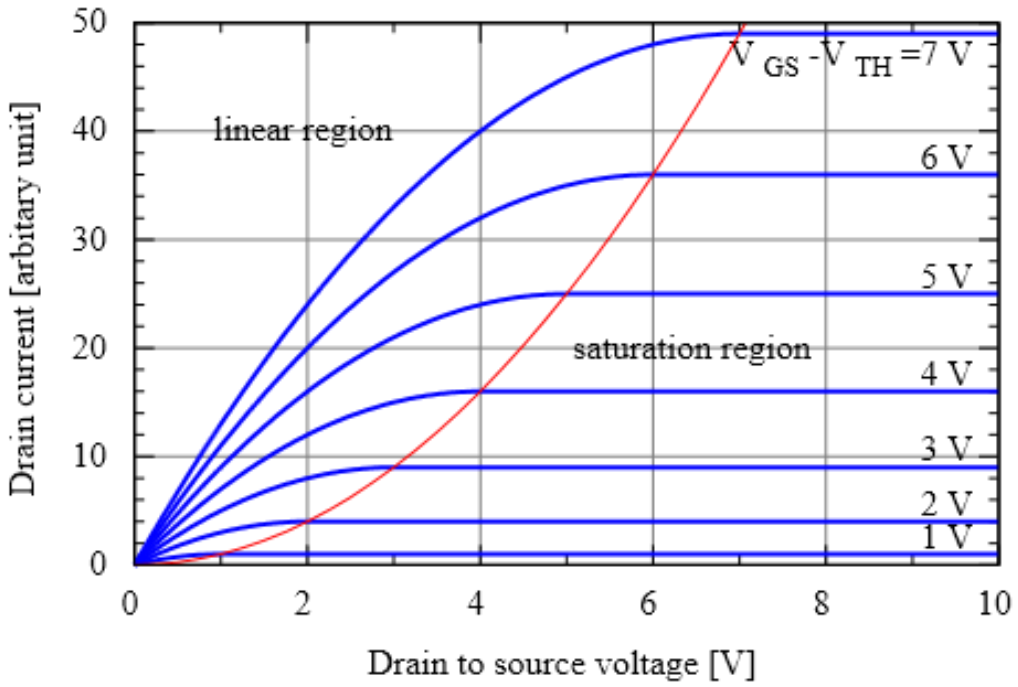

Figure 1.5.6 I_{DS}-V_{DS} output characteristics of a MOSFET

As the drain voltage increases and goes beyond the overdrive voltage ($V_{DS} > V_{GS} - V_{th}$), the drain current flattens and reaches saturation. In the saturation region, the expression for drain current becomes

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)^2$$

The transconductance of a MOSFET is a measure of the change in drain current with respect to the change in the gate voltage at a fixed drain voltage:

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}}$$

Incorporate the drain current in the linear region, we have

$$g_m = \mu C_{ox}\frac{W}{L}V_{DS}$$

From this expression, we know the transconductance is independent of the gate voltage in the linear region. It is a function of the carrier mobility, capacitance of the oxide, width and length of the channel, as well as the drain voltage.

To obtain the tranconductance experimentally, we can first measure the drain current as a function of the gate voltage, V_{GS}, at a given drain voltage. Then the transconductance is simply the slope of the linear region of that curve. We are also able to obtain the threshold voltage by extrapolating the linear region to intersect with the horizontal axis.

2. Detailed Processing Procedures

2.1 Week 1. Field Oxide Growth

2.1.1 Wafer Scribing

In this IC fab lab class, each group has a total of 12 silicon wafers, with 6 p-type ones and 6 n-type ones. In order to identify them during the multi-step fabrication process, the wafers were marked on the unpolished side using a diamond tipped scribe. The wafers were indexed using two letters followed by a number, WN(P)-X. The first letter "W" stands for Wednesday group. The second letter indicates the type of the wafer, either N or P. The last number distinguishes different wafers, ranging from 1 to 4. Note that there is a "T" in front of the number for all the test wafers.

2.1.2 RCA Clean for Wafers

The indexed wafer then underwent a Radio Corporation of America (RCA) cleaning process. It comprises 3 steps: RCA1, hydrofluoric acid (HF) dip, and RCA2. The RCA1 bath is made of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and deionized water (DIW) with a volume ratio of 1:1:5. Its purpose is to remove organic contaminants and particles from the surface. During this step, a thin layer of silicon dioxide is inevitably introduced on the silicon surface, which will be removed in the second step. The HF solution consists of hydrofluoric acid and water in a 1:20 volume ratio. A short immersion of the silicon wafers in the HF solution tends to remove the thin oxide layer and some portion of ionic contaminants. The RCA2 bath is a solution of hydrochloric acid (HCl), H_2O_2 and deionized water with a volume ratio of 1:1:5. This treatment is effective in removing metallic contaminants. Table 2.1.1 shows the detailed procedure for RCA cleaning:

Table 2.1.1 RCA clean procedure

Step Number	Step Description
1	RCA 1 for 15 min
2	Rinse in DIW for 4 cycles (~6 min)
3	HF immersion for 30 sec
4	Rinse in DIW for 4 cycles (~6 min)

5	RCA 2 for 15 min
6	Rinse in DIW for 4 cycles (~6 min)

The chemicals we deal with in RCA clean are considered reactive and thus health hazard to the users. Hence they must be handled in a fume hood and safety gears, including facial mask, apron, and chemical-resistant gloves, must be worn during RCA clean. Figure 2.1.1 shows the wet bench where the RCA clean was performed.

Figure 2.1.1 Wet bench for RCA clean.

2.1.3 Field Oxide Growth

After the RCA clean, the wafers were dried in a spin rinse dryer, and then transferred to a Bruce furnace in a quartz holder for field oxide growth. The wafers for device fabrication were placed in the middle portion of the quartz holder, while the rest four test wafers were placed at both ends to ensure better oxide growth of the device wafers. To achieve uniform thickness of field oxide across the wafer, a baffle was positioned in the chamber to induce turbulence of the incoming gases. A picture of the Bruce furnace that we used is shown in Figure 2.1.2.

Figure 2.1.2 Bruce furnace for oxide growth.

The target thickness for the filed oxide growth is set to be 1 μm. In order to reach this target, the detailed procedure as shown in Table 2.1.2 was used by following a dry/wet/dry oxidation sequences.

Table 2.1.2 Detailed procedure for field oxide growth.

Step No.	Time (min)	Temperature (C)	Gas	Description
1	0	Idle	Idle	Idle

2	90	1000	N_2	Ramp up
3	60	1000	N_2	Stabilize
4	30	1000	O_2	Dry oxidation
5	300	1000	Wet O_2	Wet oxidation
6	30	1000	O_2	Dry oxidation
7	30	1000	N_2	Anneal
8	90	Idle	Idle	Cool down

2.2 Week 2. Active Area Patterning

2.2.1 Oxide Thickness Measurement

While the target thickness of field oxide is 1 μm, there is always deviation from that target in the actual wafers. In order to determine the actual thickness of the field oxide, the wafers were measured with Filmetrics F40-UV interferometer. In an interferometer (Figure 2.2.1), the thickness of thin films is measured based on interferometry. Below is the procedure for interferometer measurement in detail.

1. Turn on the instrument.
2. Place the wafer under the microscope associated with the interferometer. Make sure the edge of the wafer is in the view.
3. Adjust both coarse and fine adjustment to focus the microscope on the wafer.
4. Move the wafer by adjusting the knob both in the front and on the right of the sample stage.
5. On the monitor, open the software. Build the material system for the thickness measurement. In our case, the first layer is silicon, and its thickness can be estimated to be 1000 μm. The second layer is silicon oxide, the thickness of which would be estimated to be 1000 ± 500 nm.
6. Take the measurement. Verify the fit of the measurement is within acceptable errors.
7. Change multiple spots and repeat step 6.

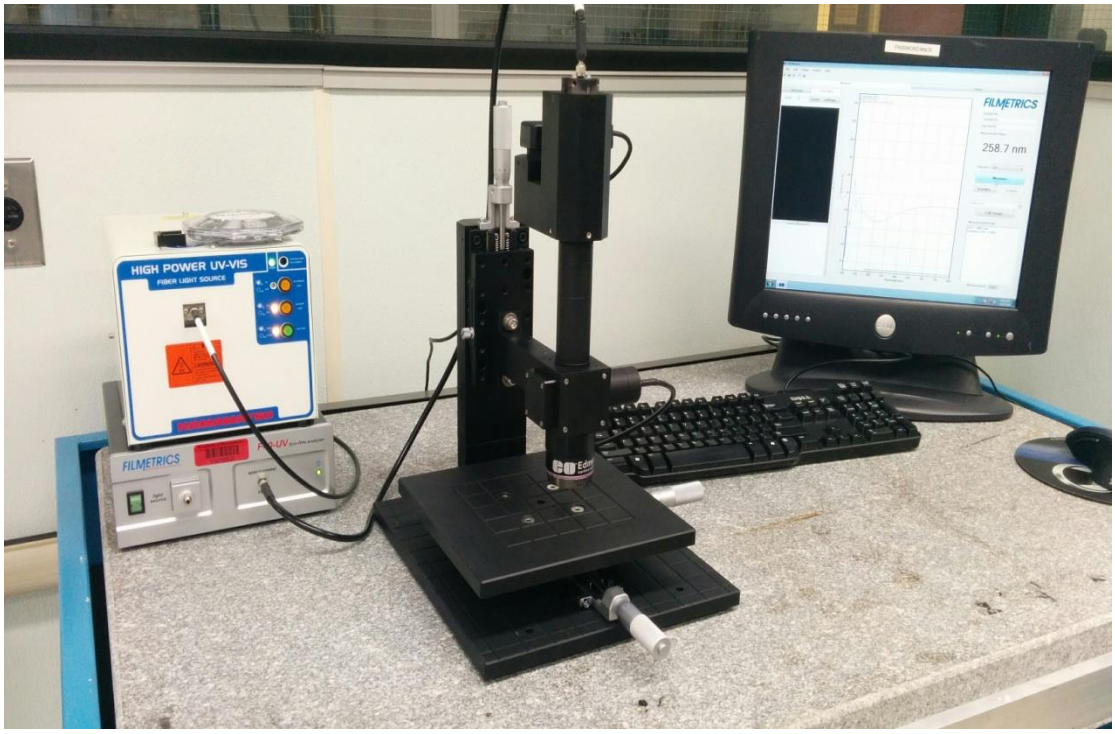

Figure 2.2.1 Filmetrics F40-UV Interferometer

The thickness of the field oxide on different wafers is presented in Table 2.2.1.

Table 2.2.1 Thickness measurement of field oxide (unit: nm)

Wafer No.	1	2	3	4	5	Average
WN-1	1013	1013	1019	1017	1016	1016
WN-2	1025	1026	1027	1028	1024	1026
WN-3	1020	1020	1019	1019	1020	1020
WN-4	1023	1021	1023	1021	1020	1022
WP-1	1019	1019	1019	1018	1019	1019
WP-2	1023	1022	1021	1021	1024	1022
WP-3	1013	1010	1007	1007	1005	1008
WP-4	1001	1002	1002	1001	1000	1001

WNT-1	1001	1002	1002	1002	1002	1002
WNT-2	1018	1018	1014	1014	1014	1016
WPT-1	994	989	989	989	988	990
WPT-2	1000	1000	1001	999	1000	1000

2.2.2 Photolithography for Active Area Patterning

The next step is to apply photolithography to each wafer except for test wafers to define the active device area. In the photolithography, two major instruments were used, including Headway photoresist spinner (Figure 2.2.2) and OAI aligner (Figure 2.2.3) for exposure.

Figure 2.2.2 Headway spinner

In general, the parameters of the spinner were set so that the final thickness of the photoresist (S1813 in our case) was about 1.7 μm. Prior to the photoresist deposition, a thin layer of hexamethyldisilazane (HMDS) was placed on the wafers to promote the adhesion between the photoresist and the wafers. After photoresist coating, a soft bake on a 100 ^{o}C hot plate for 60 sec

was applied to all the wafers to cure the photoresist so that its thickness would remain constant for further handling. The detailed procedure for photoresist coating is described below.

1. Place the wafer on spinner chuck.
2. Turn on the vacuum. Check for vacuum by tapping on the side of the wafer gently.
3. Apply HMDS onto the wafer.
4. Close the lid and start the programmed spinner.
5. Wait for 30 sec while spin coating HMDS on wafer at 3000 rpm.
6. The spinner stops for 30 sec and apply photoresist during this time window.
7. Spin coat the photoresist on the wafer at 3000 rpm for 30 sec.
8. Turn off the chuck vacuum.

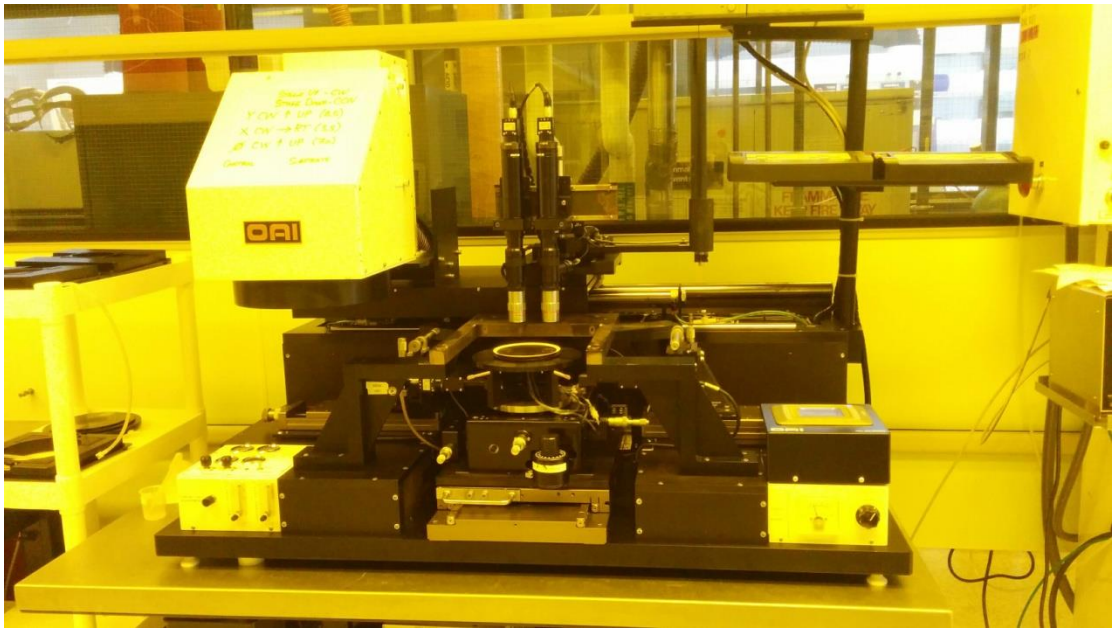

Figure 2.2.3 OAI aligner

In case the photoresist coating is not uniform across the wafer due to insufficient amount of photoresist, a re-work is needed. After placing the wafer onto the chuck, the wafer was flooded with acetone. As the spinner was turned on and the rotating speed was ramping up, spray methanol and isopropanol onto the wafer simultaneously to remove the photoresist. Make sure the wafer surface is not dry when apply methanol and isopropanol.

Once the photoresist layer with desired thickness was spun-coat on the wafers, they were transferred to an OAI aligner (Figure 2.2.3) for exposure. The active device area was defined using a mask. The procedure to use the OAI aligner is as follows:

1. Pull out the stage and place the wafer on the chuck, and make sure the major flat of the wafer is aligned with the two points at about 6 o'clock on the chuck.
2. Turn on the substrate vacuum to stabilize the wafer.
3. Push the stage all the way in while pressing down the rubber rim surrounding the chuck to prevent it from rolling up.
4. Increase the height of the chuck so as to bring the wafer in view but not in contact with the mask.
5. Bring the wafer in contact with the mask.
6. Turn on the contact vacuum.
7. Expose the wafer to UV light source for 6.0 sec. ATTN: notify people nearby of the UV exposure.
8. Turn off the contact vacuum.
9. Bring down the stage to its initial position and pull it out.
10. Turn off the substrate vacuum.
11. Take out the wafer.

After UV light exposure in the OAI aligner, the wafer was transferred to a wet bench for development by using the AZ 300 developer. The wafer was first placed into the developer for 60 sec. During this time, the solution was swirled to ensure sufficient contact between the developer and the photoresist. Then the wafer was dipped into a DI water tank for 60 sec, followed by drying with nitrogen gun.

The critical dimensions (CD) and the alignment sites on the wafer were inspected with an optical microscope. Next, the wafers were placed in an oven at 120 ^{o}C for 30 min for hard bake.

2.2.3 Field Oxide Etching

After the photolithography step, the active area for device was well-defined. In the next step, the oxide that was not covered by the photoresist needed to be removed. Buffer oxide etch (BOE, a mixture of HF and NH_4F) was used to etch the field oxide. NH_4F here is used to supply F^- and

keep the pH of the solution. It is worthwhile noting that this wet etch technique is isotropic, i.e. the etching rate is the same for different directions.

From the interferometer measurement, we know the average thickness of the field oxide is 1012 nm. The etch rate of BOE is around 0.85 nm/sec. To ensure the complete removal of the field oxide, we targeted 20 % over etch. Therefore, the overall etching time was calculated to be 23 min. Since the silicon oxide is hydrophilic while the silicon is hydrophobic, there is a simple way to qualitatively confirm the removal of oxide layer by check if water sticks to the wafer. At the end of this week, a schematic of the MOSFET is presented in Figure 2.2.4.

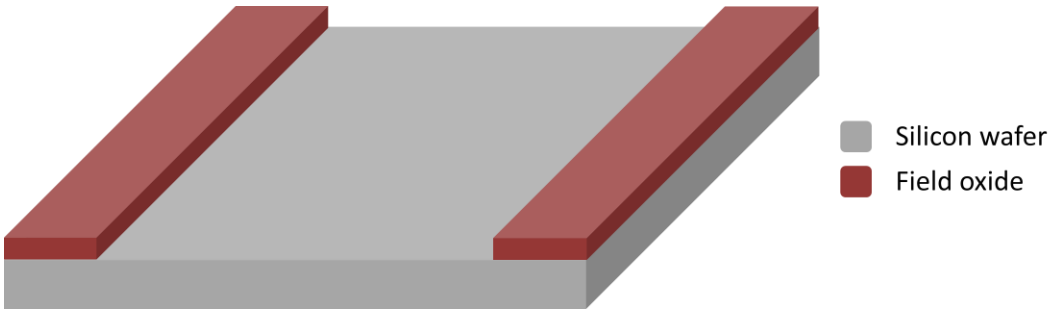

Figure 2.2.4 Schematic of a MOSFET after active area definition.

2.3 Week 3. Gate Oxide Growth and Poly-Si Deposition

2.3.1 RCA Clean for Wafers

After photolithography and BOE steps from last week, there could still be some photoresist residues and a new thin layer of oxide grown on silicon due to exposure to the air. Hence, a standard RCA cleaning was performed to remove any undesired organic and metallic contaminants. The detailed procedure is tabulated in Table 2.1.1, and it will not be repeated here.

2.3.2 Gate Oxide Growth

Following RCA cleaning, the wafers were then transferred to a Bruce furnace for gate oxide growth. The target thickness of the gate oxide is 100 nm. Different from the field oxide growth, dry oxidation was adopted here since it is capable of growing denser oxide with lower defect density and the thickness can be more accurately controlled. The trade-off is the growth rate. The growth rate of dry oxidation is approximately 10 times slower than wet oxidation. The recipe for gate oxidation is presented in Table 2.3.1. The schematic of a MOSFET after gate oxidation is shown in Figure 2.3.1.

Table 2.3.1 Detailed procedure for gate oxide growth.

Step No.	Time/min	Temperature/ ºC	Gas	Note
1	90	1050	N_2	Ramp to 1050 ºC
2	60	1050	N_2	Stabilize
3	75	1050	O_2	Dry oxidation
4	30	1050	N_2	Anneal
5	90	Idle	N_2	Cool down

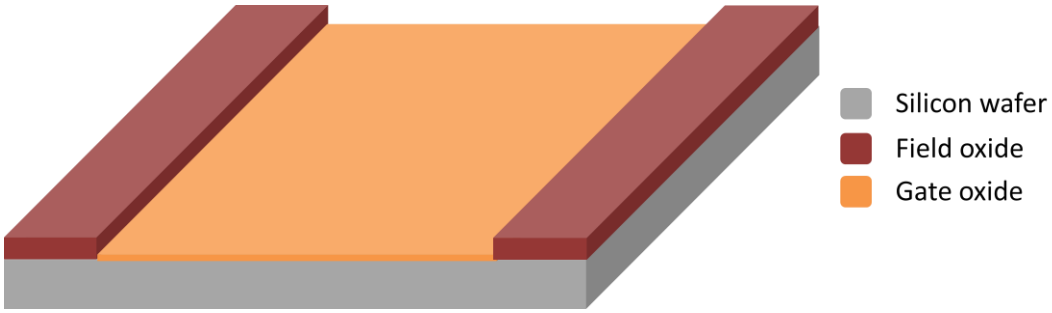

Figure 2.3.1 Schematic of a MOSFET after gate oxidation.

2.3.3 Poly-Si Deposition

After growing a thin layer of gate oxide on the wafers, they were transferred to CVC sputter for polysilicon deposition. The target is set to be 800 nm. Below is the recipe for poly-Si deposition. Figure 2.3.2 shows the schematic of a MOSFET after this step.

Table 2.3.2 Recipe for poly-Si deposition

Step No.	Time/min	Voltage/V	Current/A	Power/kW	Purpose
1	3	460	1.92	0.9	Presputter
2	60	460	1.92	0.9	Sputter

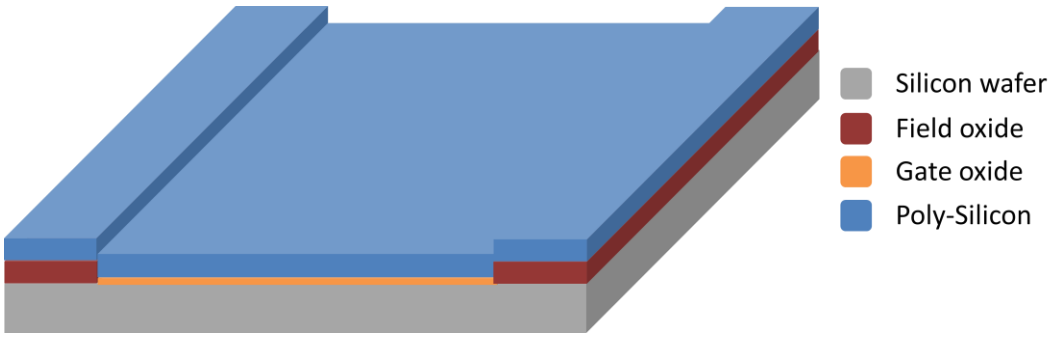

Figure 2.3.2 Schematic of a MOSFET after poly-Si deposition.

2.4 Week 4. Source and Drain Patterning

2.4.1 Gate Oxide Measurement

Our target for gate oxide is 100 nm. The actual thickness was measured by Filmetrics F40-UV interferometer following the procedure described in section 2.2.1. The measurement was performed on the test wafer WNT-2, and the five sets of thickness we measured were 108 nm, 109 nm, 107 nm, 109 nm, and 108 nm, respectively, giving an average of 108 nm.

2.4.2 Photolithography for Source/Drain Patterning

In order to define the source and drain area, the poly-Si needs to be etched away except for the gate area. Therefore, photolithography was applied for the second time with M2 mask. Each wafer except for the test wafers went through the photolithography procedures described in section 2.2.2. In this step, there would be overlay of M2 mask with M1 mask. It is important to ensure the M2 mask is in good alignment with the underlying active device area defined by the first photolithography. To achieve this, the x, y, and the angle θ must be carefully adjusted to align with the Vernier scale. Upon bringing the wafer in contact with the mask, the x, y and θ values should all within 5 μm to be considered as in specification. Otherwise, the wafer needs to be separated from the mask and alignment must be performed again.

After going through spin coating, exposure, development, the wafers were placed under an optical microscope to verify the exposure time was neither too short (under exposure) nor too long (over exposure) and that the patterns were in specification. Then the wafers were transferred to an oven at 120 ^{o}C for 20 min to cure the photoresist.

2.4.3 Reactive Ion Etching

Next, the poly-Si not covered by photoresist was removed with reactive ion etch (RIE). In our experiment, an Adixen AMS 100 etcher, as shown in Figure 2.4.1, was used in this step. Following is the recipe for RIE. A schematic of the MOSFET after this step is shown in Figure 2.4.2.

Table 2.4.1 Recipe for RIE

Time/sec	Pressure/mbar	Gas	Flow/sccm	ICP power	RIE power
45	4.5×10^{-2}	SF_6	300	1800	40

Figure 2.4.1 Adixen AMS 100 reactive ion etcher.

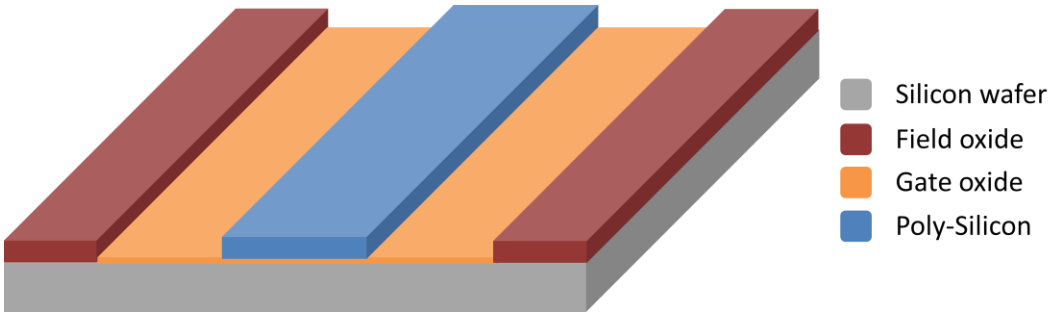

Figure 2.4.2 Schematic of a MOSFET after poly-Si etch.

2.4.4 Ion Implantation

After poly-Si etch, all the wafers were sent to California for source and drain ion implantation. For NMOS, arsenic (As) was used for doping using an implant energy of 150 keV. On the other hand, PMOS were doped with boron (B) using an implant energy of 50 keV.

2.5 Week 5. Deposition and Densification of Inter-Level Dielectric (ILD)

2.5.1 Caro's Etch and BOE

Prior to inter-level dielectric (ILD) deposition, it is necessary to remove the contaminants, including organics and coarse particulates, using Caro's etch or Piranha etch. The procedure goes as follows:

1. Rinse the quartz container with DI water and place it inside the hood.
2. Mix H_2O_2 and H_2SO_4 in a 1:1 volume ratio, 2 L each. Pour H_2SO_4 into the container first.
3. Load all the wafers onto a Teflon rack and place it in the Piranha solution for ~10 min.
4. Rinse the wafers in DI water.
5. Spin rinse and dry the wafers.

Following Caro's etch, a BOE was performed to remove the residual gate oxide in the source/drain area and other oxide produced by Caro's etch. It is worthwhile mentioning that the etch rate would be larger than 0.85 nm/sec for the oxide due to the damage caused by ion implantation.

2.5.2 ILD Deposition

The ILD deposition processes are different for NMOS and PMOS. For NMOS, 1 μm of oxide layer was deposited onto the wafer by using plasma enhanced chemical vapor deposition (PECVD). This step was performed in an AMAT P5000 TEOS PECVD system. Tetraethyl

orthosilicate (TEOS) was used as precursor and source of silicon. It decomposed and reacted with oxygen to form an oxide layer on the surface. The parameters for ILD deposition on NMOS are listed below.

Table 2.5.1 Parameters used for PECVD on NMOS

Time/sec	Temperature/^{o}C	Pressure/torr	Gas	Flow Rate/sccm	Power/W
115	400	9	TEOS/O_2	425/325	350

For PMOS, a 100 nm Si_3N_4 layer was first deposited onto the wafers in a Plasmatherm by following the recipe described in Table 2.5.2.

Table 2.5.2 Recipe for Si_3N_4 deposition in a Plasmatherm.

Step No.	RF/W	Pressure/torr	Step Time/min	Gas	Description
1	0	0	1	None	Pump
2	0	0	1.5	50% of N_2, 50% of 2% SiH_4 in N_2	Set MFC
3	0	1	2	50% of N_2, 50% of 2% SiH_4 in N_2	Pressure
4	167	1	5.6	50% of N_2, 50% of 2% SiH_4 in N_2	Deposit
5	0	0	1	None	Pump
6	0	0	1.5	50% of N_2, 50% of 2% SiH_4 in N_2	Purge
7	0	0	1	N_2	Pump

Another 900 nm of ILD was then deposited on top of the nitride layer using the following recipe.

Table 2.5.3 Parameters used for ILD deposition on PMOS

Time/sec	Temperature/^{o}C	Pressure/torr	Gas	Flow Rate/sccm	Power/W
95	400	9	TEOS/O_2	425/325	350

2.5.3 ILD Densification

When the ILD deposition on both NMOS and PMOS was completed, the wafers were transferred to a Bruce furnace for densification annealing. Below are the recipes for ILD densification for both NOMS and PMOS.

Table 2.5.4 Recipe for ILD densification of NMOS.

Step No.	Time/min	Temperature/^{o}C	Gas	Description
1	60	600	N_2	Ramp up
2	20	1000	N_2	Densification
3	360	600	N_2	Densification
4	60	200	N_2	Cool down

Table 2.5.5 Recipe for ILD densification of PMOS.

Step No.	Time/min	Temperature/^{o}C	Gas	Description
1	60	600	N_2	Ramp up
2	20	900	N_2	Densification
3	360	600	N_2	Densification
4	60	200	N_2	Cool down

2.6 Week 6. ILD Patterning for Metal Contacts

2.6.1 Thickness Measurement of ILD after Densification

The thickness of ILD was measured using Filmetrics F40-UV interferometer after densification. It is expected that the film thickness would be smaller than the target to some extent due to removal of voids inside the film during the annealing. The actual thickness of ILD on both NMOS and PMOS is shown in Table 2.6.1.

Table 2.6.1Thickness of ILD layer after densification (unit: nm)

Type	Material	1	2	3	4	5	Average
NMOS	SiO_2	896	896	889	891	892	893
PMOS	SiO_2	782	772	777	778	779	778
	Si_3N_4	146	147	143	142	142	144

2.6.2 Photolithography for ILD Patterning

Photolithography was applied to the wafers to define the metal contact area. Briefly, photoreisist was spun-coat onto the wafer at 3000 rpm for 30 sec, which resulted in a 1.7 μm photoresist layer. Then the wafer was placed on a 100 ^oC hot plate for 60 sec of soft bake. After that, the wafer was loaded into the OAI aligner for photoresist exposure. M3 mask was used for this step. Again it is important to have the mask well-aligned with the underlying pattern by adjusting the x, y and θ deviation. The wafer was next immersed into developer for 60 sec, followed by DI water rinsing and drying. In the end, a 30 min hard bake at 120 ^oC was performed in an oven.

2.6.3 ILD Etching

The Plasmatherm system (see Figure 2.6.1) was first used to etch ILD on both NMOS and PMOS owing to its anisotropic etching and fast etching rate. A mixture of CHF_3 and O_2 was used to etch away both oxide and nitride layers. The etching rate for oxide and nitride were 22 nm/min and 38 nm/min, respectively. The recipes for ILD etch on NMOS and PMOS were slightly different since it took longer to etch 1 μm of oxide than 100 nm nitride and 900 nm oxide. The procedure for ILD etch was tabulated in Table 2.6.2.

Table 2.6.2 Procedure for ILD etching

Step No.	RF/W	Pressure/torr	Step Time/min	Gas	Description
1	0	0	1	None	Pump
2	0	0	1.5	45% of CHF_3, 5% of O_2	Set MFC
3	0	0.03	2	45% of CHF_3, 5% of O_2	Pressure
4	167	0.03	45 min (NMOS) 38 min (PMOS)	45% of CHF_3, 5% of O_2	Deposit
5	0	0	1	None	Pump
6	0	0	1.5	50% of N_2	Purge
7	0	0	1	None	Pump

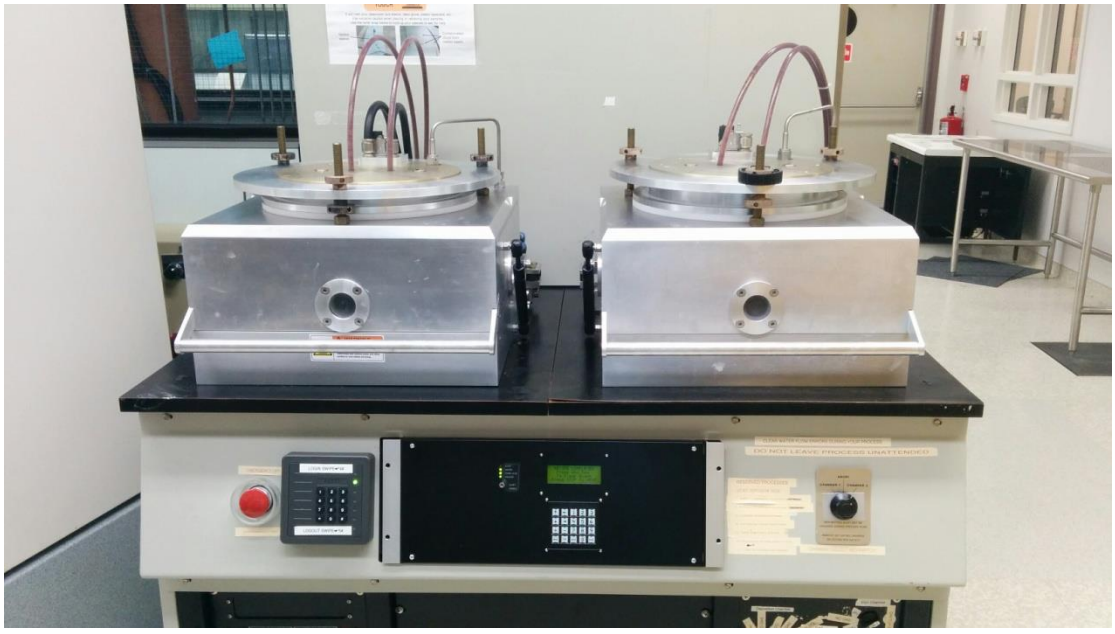

Figure 2.6.1 Plasmatherm system (including PECVD and RIE etcher)

2.6.4 Post RIE etch and Photoresist Stripping

In the prior step, the oxide and nitride were not completely removed. Interferometer measurement showed that the thickness of the residual layer on NMOS was about 70 nm. All the wafers were subject to a buffered oxide etch (BOE) for 70 sec for complete oxide removal. However, the nitride would not be etched by BOE. Any remaining nitride layer would eventually prevent good metal contact to the sour/drain area and thus make the PMOS not working. In fact, none of our PMOS worked properly. And this is the primary reason for that.

In the end, the residual photoresist were removed by immersing the wafers in the stripper for 10 min at 60 ^{o}C. The schematic of a MOSFET after this week is presented in Figure 2.6.2.

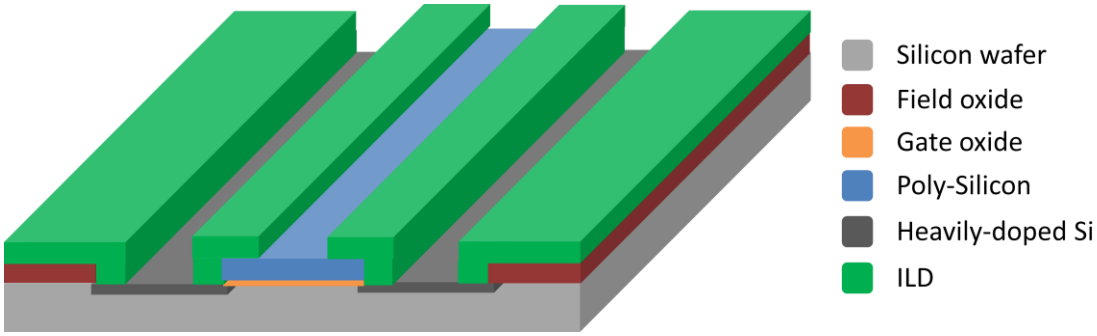

Figure 2.6.2 Schematic of a MOSFET after ILD patterning.

2.7 Week 7. Metallization

2.7.1 Native Oxide Etch

Prior to aluminum (Al) sputtering, BOE was performed on the wafers for 20 sec to remove any native oxide at the contact area. The wafers were then dried before transferring into a sputter tool. Note that this step was completed by clean room staff.

2.7.2 Aluminum Sputtering

Sputter deposition is a physical vapor deposition (PVD) method for depositing thin films. In sputtering, the material from a target, whether metal or dielectric, was knocked off and then deposited onto a substrate, such as a silicon wafer. A DC sputtering system was used for Al deposition, as shown in Figure 2.7.1.

If pure Al was deposited onto the wafer, the Al atoms could easily diffuse into the underlying silicon layer, especially under high temperature conditions, which leads to the formation of spikes. These spikes are detrimental to the devices and they need to be prevented. In order to fulfill this goal, an aluminum target with about 1% silicon was chosen for sputter deposition.

Figure 2.7.1 Top: Overview of the sputter tool. Bottom: Inside view of the sputter tool.

2.7.3 Aluminum Patterning

A fourth photolithography was applied here for aluminum patterning. Please refer to section 2.2.2 for detailed procedure. The alignment among different masks was inspected with an optical

microscope. If the misalignment was within 5 μm, the wafers were hard-baked in an oven at 120 ^{o}C for 20 min.

2.7.4 Aluminum Etch

The aluminum uncovered by the photoresist was removed by a mixture solution of H_3PO_4, H_2O, CH_3COOH and HNO_3 (volume fraction 80:10:5:5) at ~50 ^{o}C. In this mixture, H_3PO_4 was used to etch aluminum oxide (Al_2O_3), was HNO_3 used to etch Al, and CH_3COOH was used to increase the selectivity. The completeness of the Al etch was determined by the bubbling rate from the wafer surface. Initially, the reaction between the solution and the Al was violent, generating lots of bubbles. As the reaction continued, the bubbling rate decreased. At last, there were only few bubbles coming out from the surface, at which point the Al etch was considered finished. The schematic of a MOSFET after this week is presented in Figure 2.7.2.

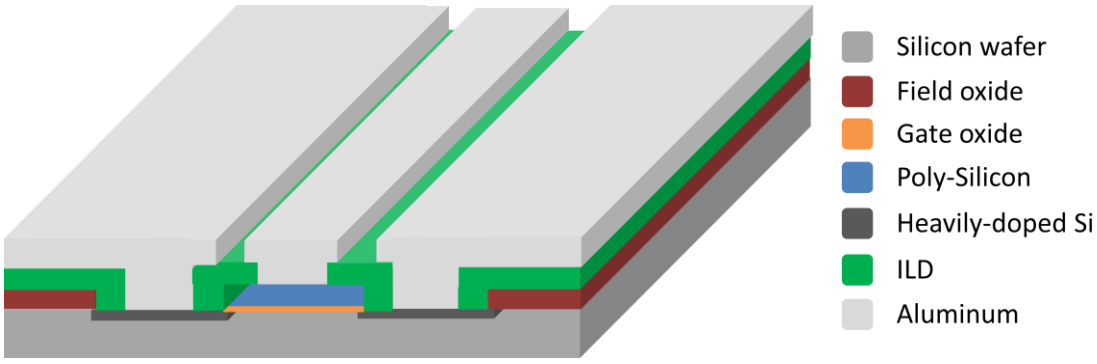

Figure 2.7.2 Schematic of a MOSFET after metallization and etch.

2.8 Week 8. Backside Metal Contact

The backside metal contact was performed by the clean room staff.

Briefly, photoresist was spun-coat on the wafers to form a passivation layer to protect the devices during backside metallization. Photoresist exposure was not necessary here. After that, BOE was performed on the backside of the wafer for 60 sec to remove the oxide. Next, aluminum with 1% of silicon was sputtered onto the backside of the wafers using a DC sputtering process described in section 2.7.2. The photoresist were removed in the stripper before the backside metal films were sintered at 400 ^{o}C for 20 min in a forming gas atmosphere (3% H_2 in argon). The final structure of a MOSFET is schematically drawn in Figure 2.8.1. The image of a complete die on

the wafers is shown in Figure 2.8.2, and it is easy to find various devices on it, including linear and circular MOSFETs, MOS capacitors, transmission lines, van der Pauw structure, Kelvin structure.

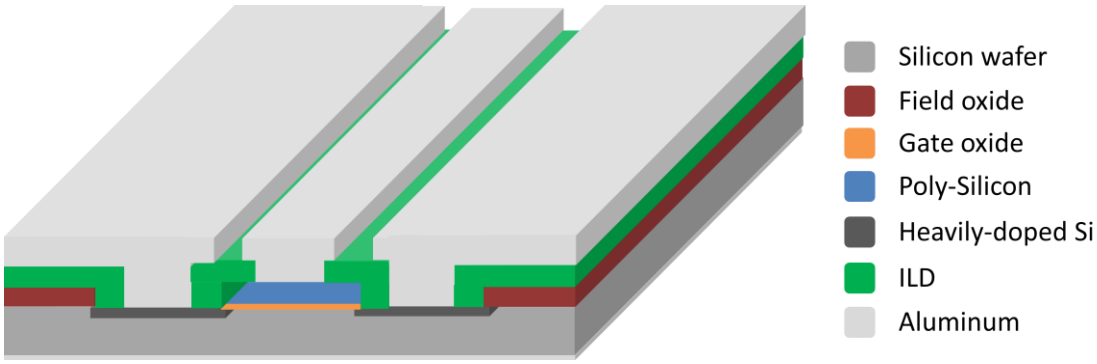

Figure 2.8.1 Schematic of a MOSFET after backside metal contact.

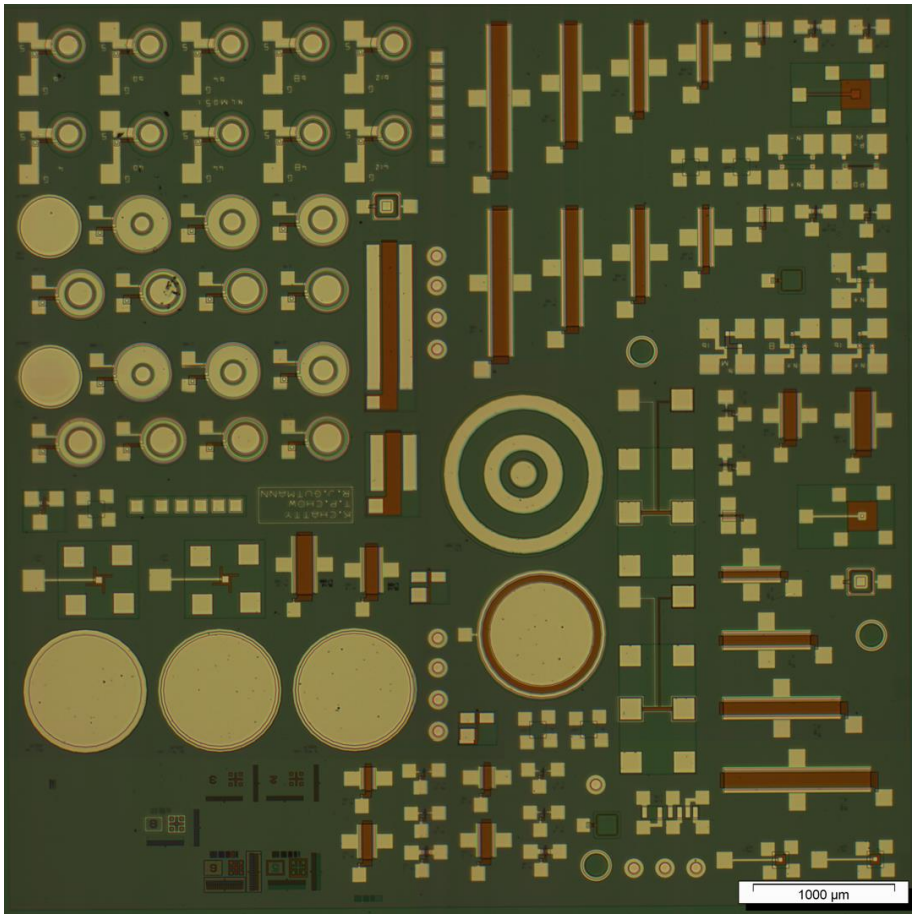

Figure 2.8.2 Optical image of complete die after fabrication.

3. Electrical Testing

3.1 Contact Measurements

Contact measurements were done to determine the contact resistance of the metal contacts. The first structure that data was taken on was the transmission line using the TLM measurement discussed in section 1.5.1.

3.1.1 Transmission Line:

These are the values extracted from the graphs that are included below for PMOS and NMOS wafers. The method of extraction has been explained in section xx.

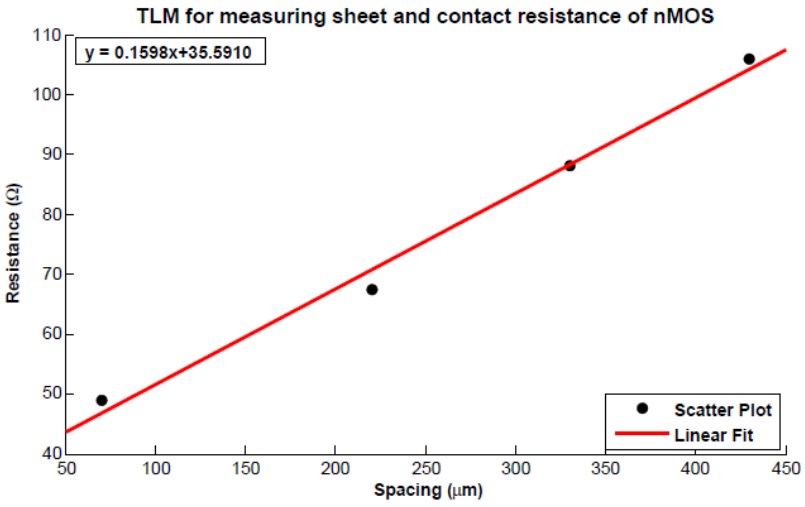

Figure 3.1.1 TLM plot for nMOS

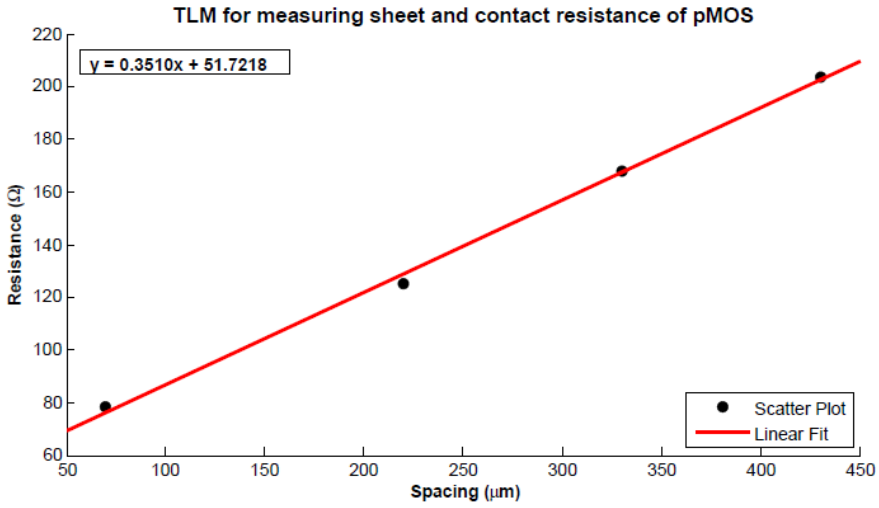

Figure 3.1.2 TLM plots for pMOS

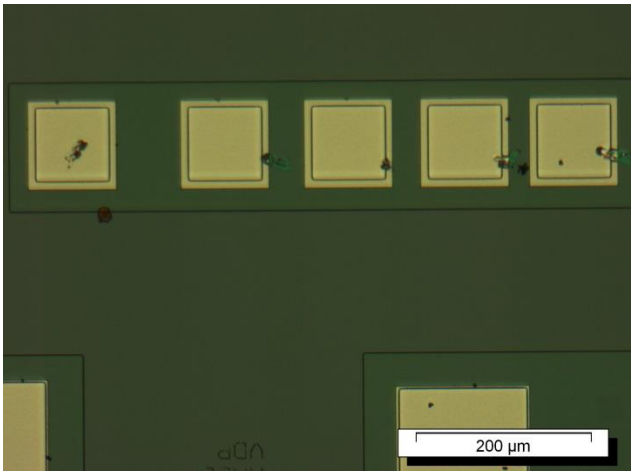

Figure 3.1.3 Transmission line structure used for testing

Table 3.1.1 Sheet resistance and Contact resistance results from TLM

Substrate	Sheet resistance (Ω/sq)	Contact resistance (Ω)	Contact resistivity (Ω-cm2)
n-MOS	0.159	17.8	2.2*10^-4
p-MOS	0.351	25.86	3.7*10^-4

3.1.2 Kelvin Structure:

The image below show the 4 Kelvin structures that were tested including the contact dimension and doping type. The contact resistance measured was between the Poly-Si and the Si substrate. As explained above, using the 4 point probes, we can generate an I-V curve, or get average

resistance and plot that. We got the resistance value from the KEITHLY machine and an example of this can be seen in Figure 3.1.4.

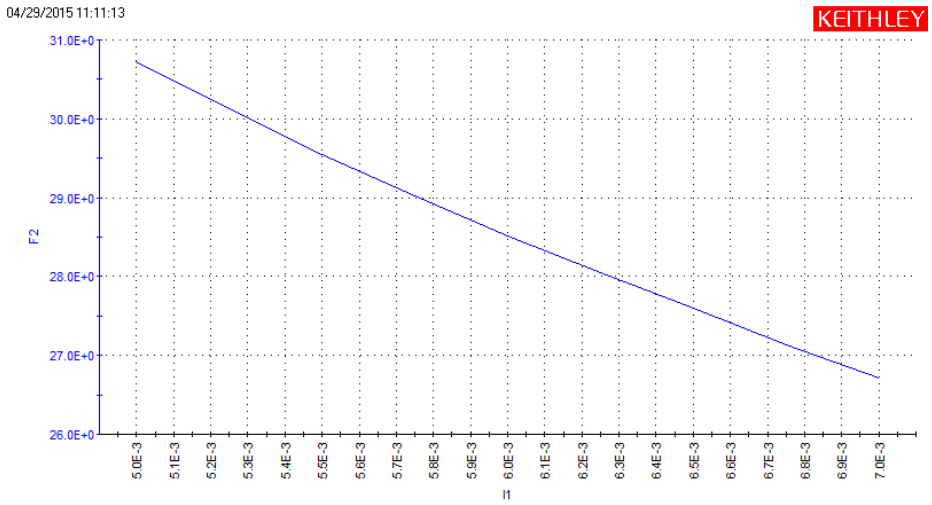

Figure 3.1.4 Example of resistance plot

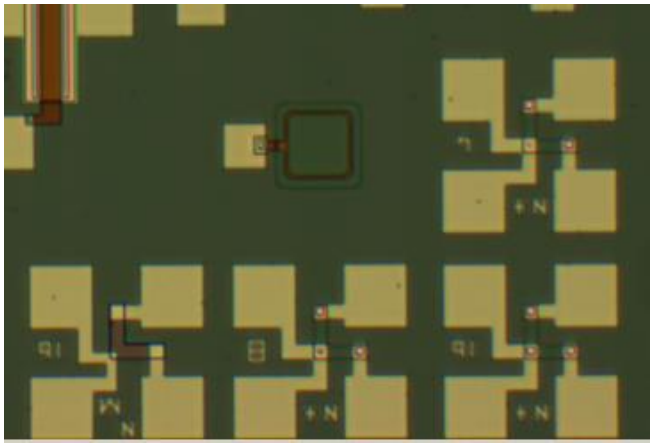

Figure 3.1.5 Structure used for testing

Table 3.1.2 Sheet resistance and Contact resistance results from TLM

	Contact resistance (Ohm)	Contact resistivity (Ohm-cm^2)	Standard deviation among wafers
nMOS 4x4	44.41	7.0*10^-6	1.19
nMOS 8x8	22.63	1.5*10^-5	0.15
nMOS 16x16	9.6	2.5*10^-5	0.04

pMOS 4x4	34.77	5.6*10^-6	--
pMOS 8x8	24.39	1.6*10^-5	--
pMOS 16x16	11.97	3.0*10^-5	--

The smaller the contact, the smaller the contact resistivity, and this can be explained by a phenomenon known as current crowding. At the contact edge the current flowing out is significant, but as we move away from the edge, the current flow drops off until there is no current.

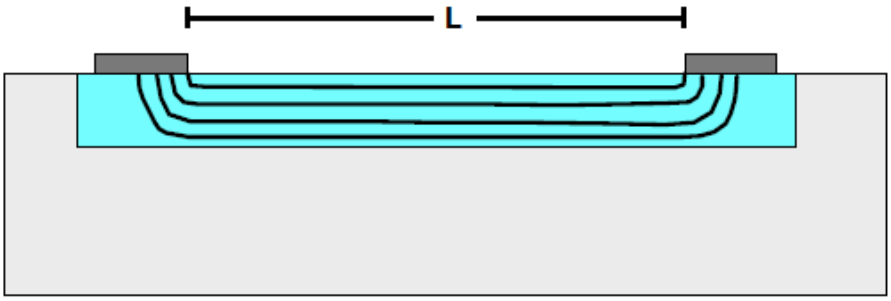

Figure 3.1.6 current crowding phenomenon

3.2 Sheet Resistance

The VdP method for measuring sheet resistance and the results are presented below. Due to the symmetric nature of our VdP structure, our geometric factor is piln/2. Table xx shows the average resistance of each pad dimensions for nMOS and PMOS. An example of VdP structure measured is seen in Figure 3.2.1. A lot of data points were taken to remove faulty readings. 4 VdP structures on 4 different die on 4 different nMOS wafers and 1 pMOS wafer.

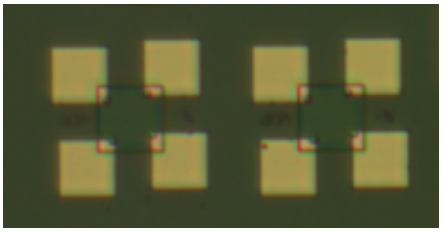

Figure 3.2.1 Van der Pauw structure used for testing

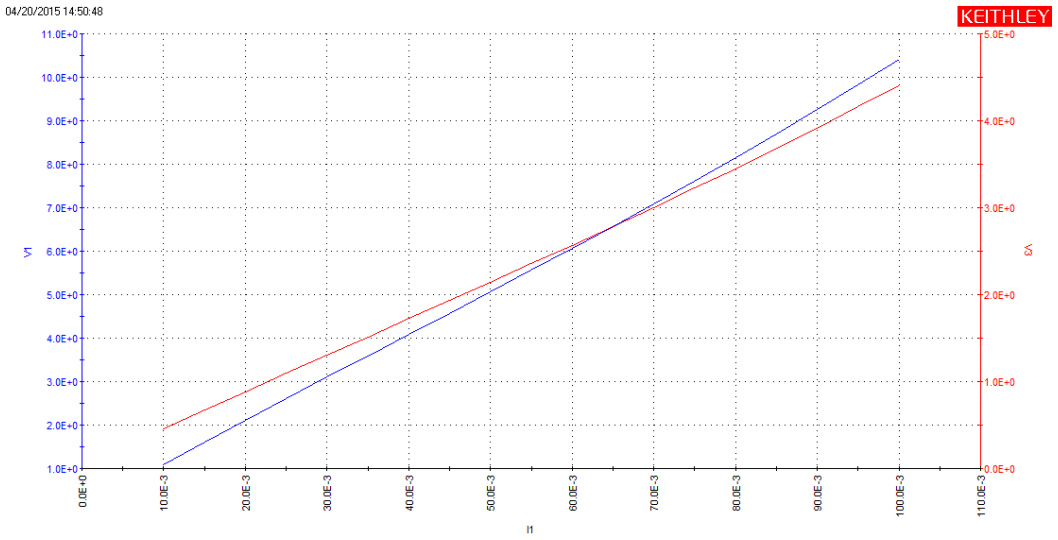

Figure 3.2.2 characteristic plot of a VdP measurement

Table 3.2.1 Sheet resistance results fromVdP structure measurements

Wafer	Avg Resistance	Sheet Resistance (Ohm/square)	Standard deviation among wafers
nMOS	8.26	37.1	1.4
pMOS	29.5	133.4	--

The hand calculated values of the sheet resistance was done using the formula given below:

$$Rs = \frac{\rho}{t}; \quad \rho = \frac{1}{\sigma}; \quad \sigma = (\mu_n n + \mu_p p)$$

The value was found to be approx. 40 ohm/square for the nMOS and 155 ohm/square for the pMOS which is not that much different from our values. This shows that the VdP testing is better for determining Sheet resistance.

3.3 NMOS IV Characterization

The two figures below show the standard operation of a linear device and a circular one on an NMOS device. Simple observation, before we get into any rigorous analysis can show some useful data between them. The first is the leakage current being significantly higher on the linear device. While this can be partially attributed to the size of the device, it is also due to edge

leakage of the linear device. Both devices have a turn on voltage between 0-1 volts. They also have a different transconductance from looking at the gaps between voltage curves. We will go on to show these assertions to be true using further analysis of the data. All analysis is done in Mathematica.

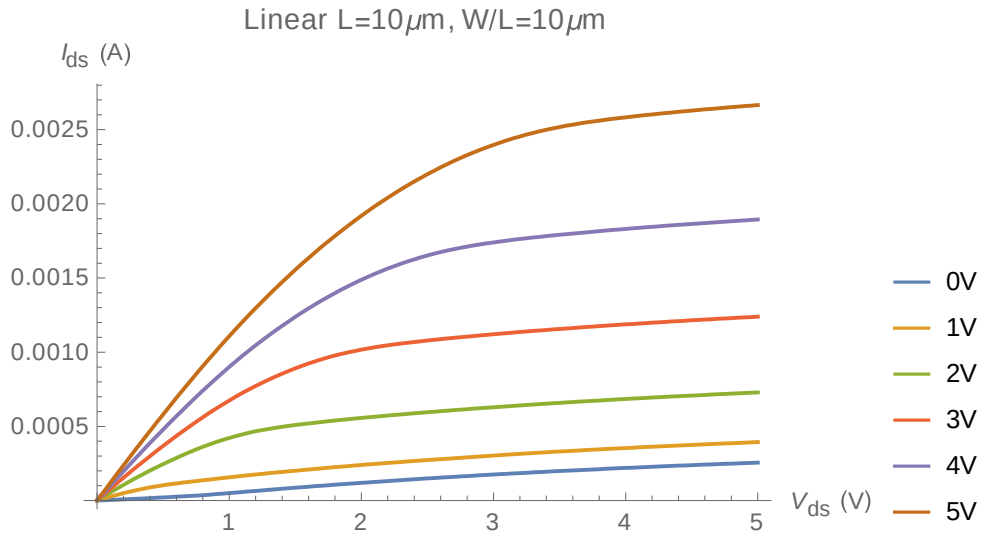

Figure 3.3.1:Vds-Ids curves of L10, WL10 linear

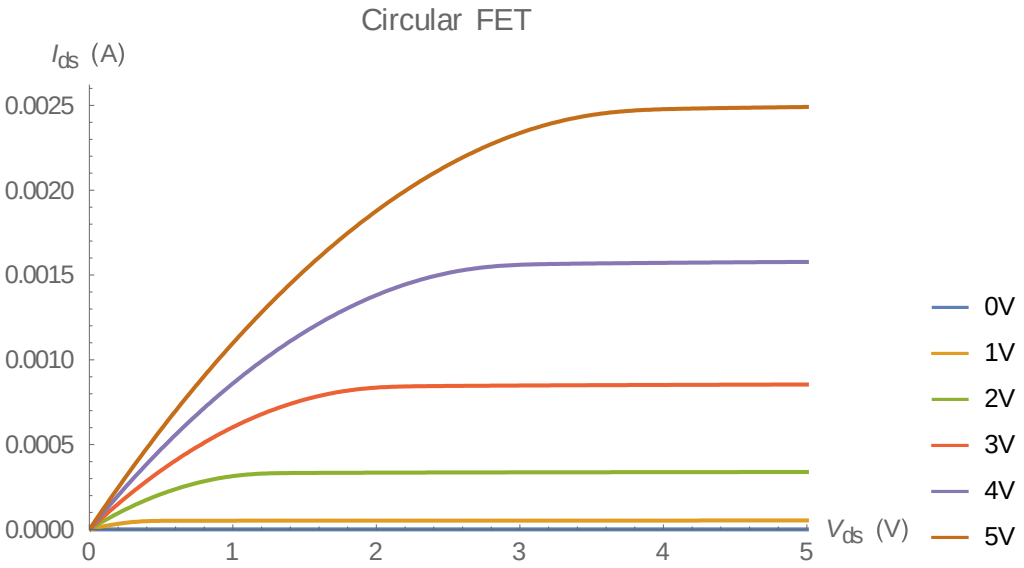

Figure 3.3.2: Vds-Ids Curves of CFET L10

3.3.1 Parallel Resistance

The next graph shows the effective parallel resistance, and thus the expected leakage current, for linear devices of WL=2 and L=2,10, and 100µm. This data is from positive values of V_{DS}, with V_{GS} below the threshold voltage. These values are all close and save for the low voltage

effects unrelated to device shape; coming in around 18kΩ, save for a slight peak at the beginning due to a gate like effect from the positive trapped charges in the oxide. This peak is minimized in the largest device. When dealing with the Circular FET, the plot is almost nonsensical at first glance. It turns out that the current flow is barely at the edge of measurement for the tools used, and thus the offset error of ~10^{-9}A is the dominant value, and the resistance is practically infinite, thus causing the increase in slope in resistance, and proving the point about leakage made from looking at the straight $V_{GS}I_{GS}$ curves. In further work this leakage current is discounted by subtracting out the current when the device is in an off state (or at least as off of a state as it can be).

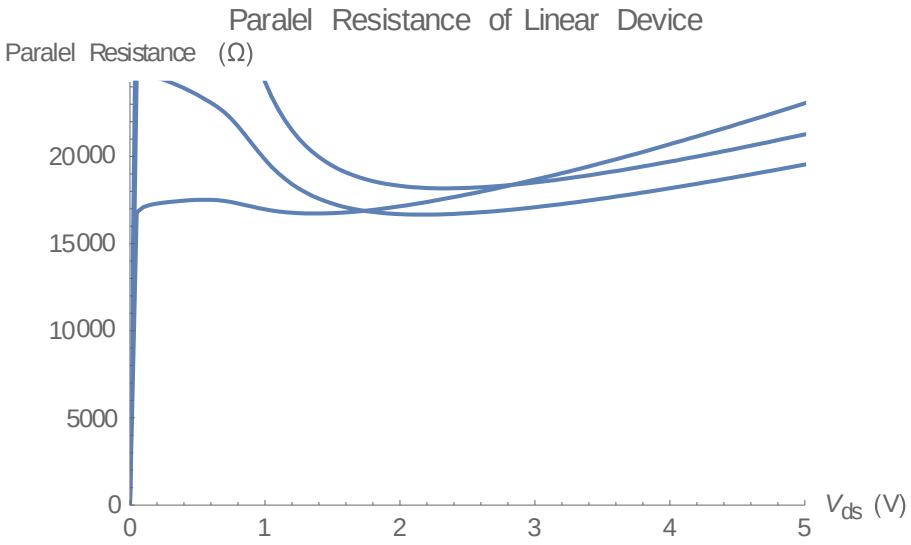

Figure 3.3.3: Parallel Resistance of Linear Device

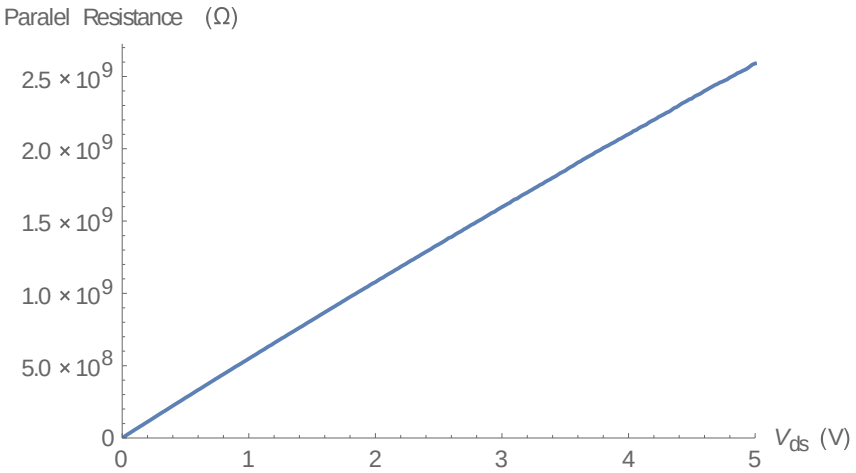

Figure 3.3.4: Parallel Resistance of Circular Device

3.3.2 Channel Length Modulation

Leakage current is not the only reason for the slopes after the device reaches saturation however; if we remember the characteristic equation for the saturation region, $I_{Dsat} = \mu_n C_{ox} \frac{W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$[10], we still have a term that depends on V_{DS}, though we have to figure out what λ is in order to determine how much of an effect it is having on our data. In the below graph, Figure 3.3.1.5, you can see the channel length modulation values by length of the device, proving the reasoning that a shorter device will have a greater effect from channel length modulation. The values range from $0.005V^{-1}$ on the 100µm devices to $0.031\ V^{-1}$ on the 2µm devices. The line is the best fit for λ to L, being a square root fit of $0.031\text{-}0.0030\sqrt{L}$. The fit is quite good, at an r^2 value of 0.98. The second figure below, 3.3.1.6, shows tracing the slope of the modulation and by tracing back and taking 1/|V| at the intercept the value of λ is found.

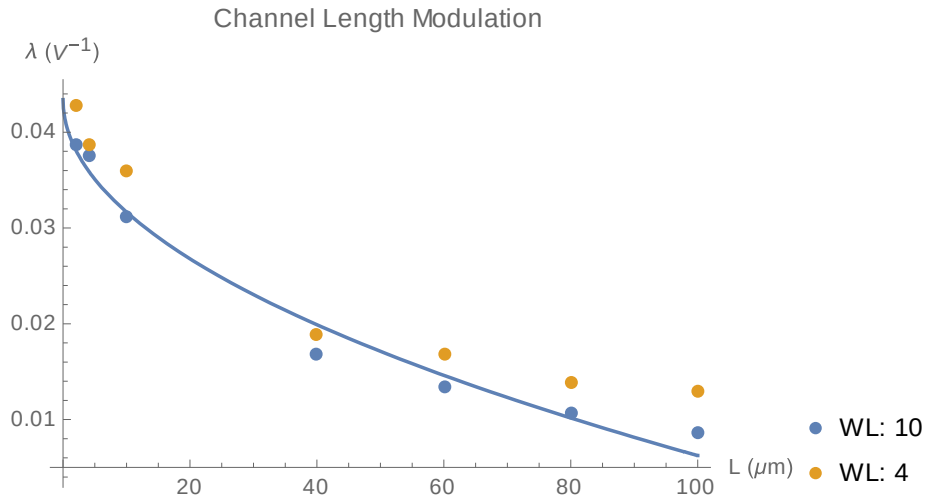

Figure 3.3.5: Channel Length Modulation Analysis

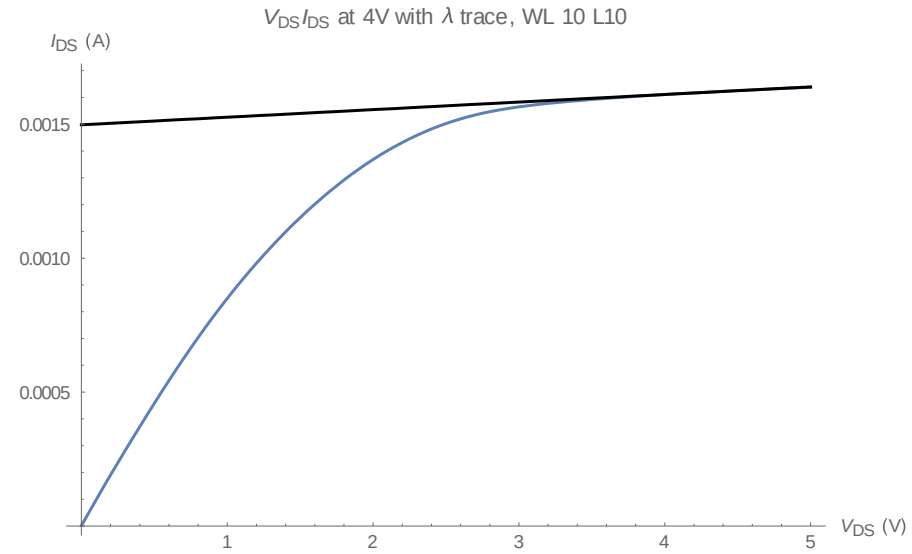

Figure 3.3.6: Channel Length Modulation Example

3.3.3 V_T Extraction

At this point there is only one more bit of useful data we can pull out of the $V_{DS}I_{DS}$ curves for a solid mathematical model of the device function, but first we have to take a detour through $V_{GS}I_{DS}$ territory. Figure 3.3.1.7 below shows the general graph of this curve for a W=10µm, W/L = 10 transistor, with the channel biased at 10mV across. It further has the first of two types of analysis to extract the threshold voltage (V_T): extrapolation in linear region. This works via finding the maximum transconductance (slope), and drawing a line tangent to that point. V_T is then equal to that point plus one half of the applied gate voltage. This method has the downside that parasitic resistances and mobility degradation can cause significant deviations from straight line behavior, as can be seen in figure 3.3.1.7.[11] In order to double check, V_T was also analyzed with the second derivative method. In this method, we find the maximum of the second derivative of the voltage (the derivative of g_m), and call that V_T. In ideal devices, this derivative would be an impulse, and thus while it is not quite one in reality, it approximates it. However, this is extremely sensitive to measurement noise due to the second derivative of collected data. This can be seen in figure 3.3.1.8 below. When analyzing the results, the ELR and SD methods had significantly similar values of V_T, of 0.067 and 0.068 respectively. ELR had a lower standard deviation of 0.031 instead of 0.036, so the value of V_T from ELR will be used.

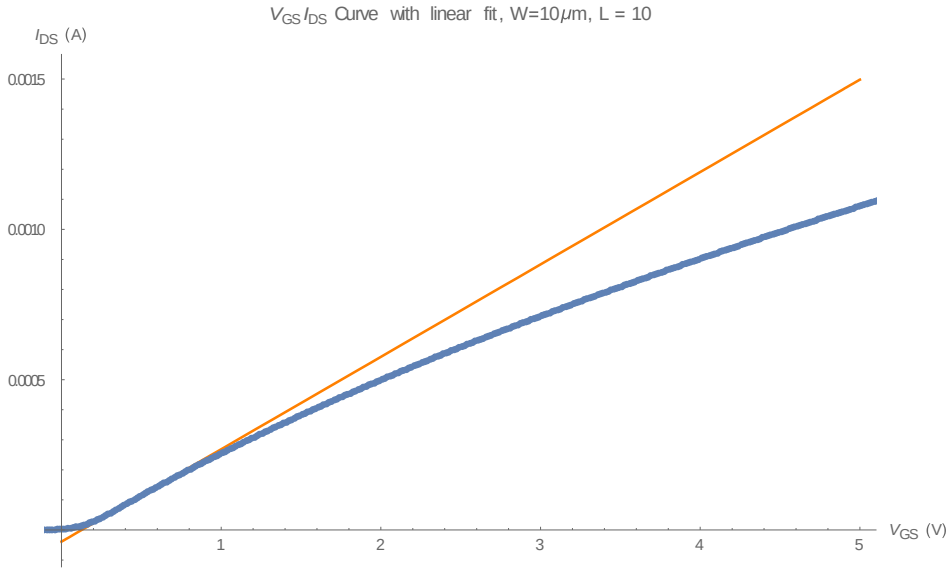

Figure 3.3.7: VGSIDS of W:10 W/L:10

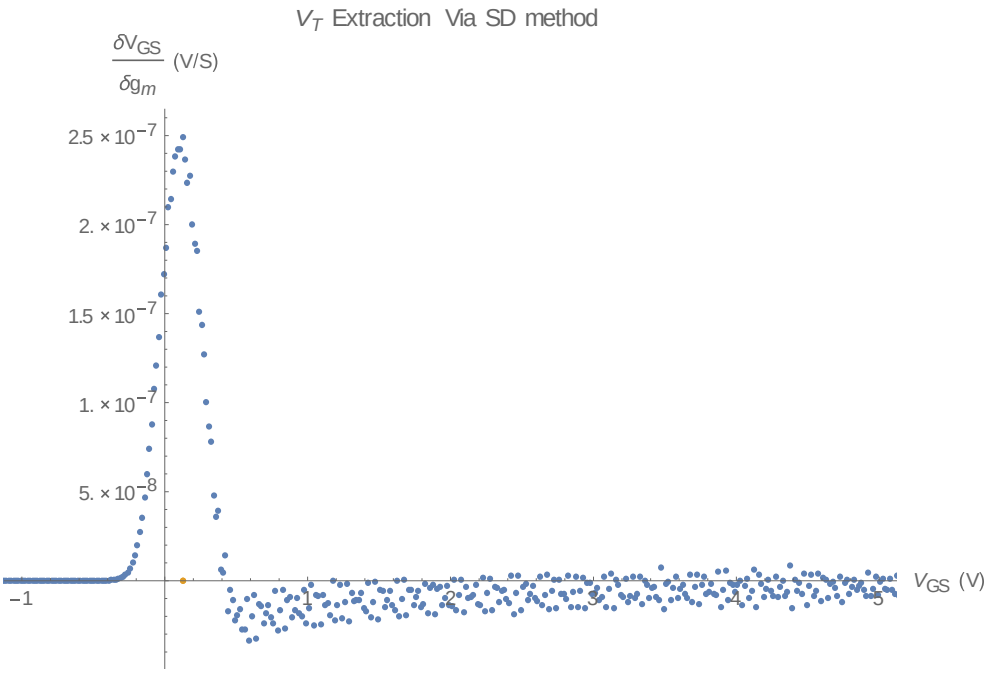

Figure 3.3.8 SD method extraction

3.3.4 μ_n and C_{ox}

Now that we have V_T, we can extract $\mu_n C_{ox}$, also known as k. While this value is useful by itself for mathematically modeling the device, we can also get the mobility once we pull the value for C_{OX} out of the capacitance measurements. Those together can be used to find μ_n, the carrier mobility. At this point, to pull k out we simply need to take a point in the saturation region from any working device and throw it into $I_{Dsat} = k\frac{W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$, ands solve for k. We get a result of $22.0*10^{-6}\frac{F}{Vs}$.

3.3.5 Table of Extracted Values

Table 3.3.1: Extracted NMOS Values

Parameter	Value or Equation
Parallel Resistance	18.7±2.4 kΩ
λ	$0.031 - 0.0030\sqrt{L}$ V^{-1}
V_T	0.067±0.031V
$\mu_n C_{ox}$	$22.0\pm0.008*10^{-6}\frac{F}{Vs}$
μ_n	690 cm^2/Vs

3.4 PMOS IV Characterization

Now to go through the same information as above, but for a different wafer, looking at PMOS devices. We had a more limited set of data for the P wafers, as ours failed as explained in section 3.11. The first bit of data that can be noted from our graphs is the movement to the third quadrant. If one looks more closely, they can also see that we do not have the leakage on the linear device to nearly the extent we had it on NMOS. This is due to the oxide charges being positive, and thus not causing a P channel in this device.

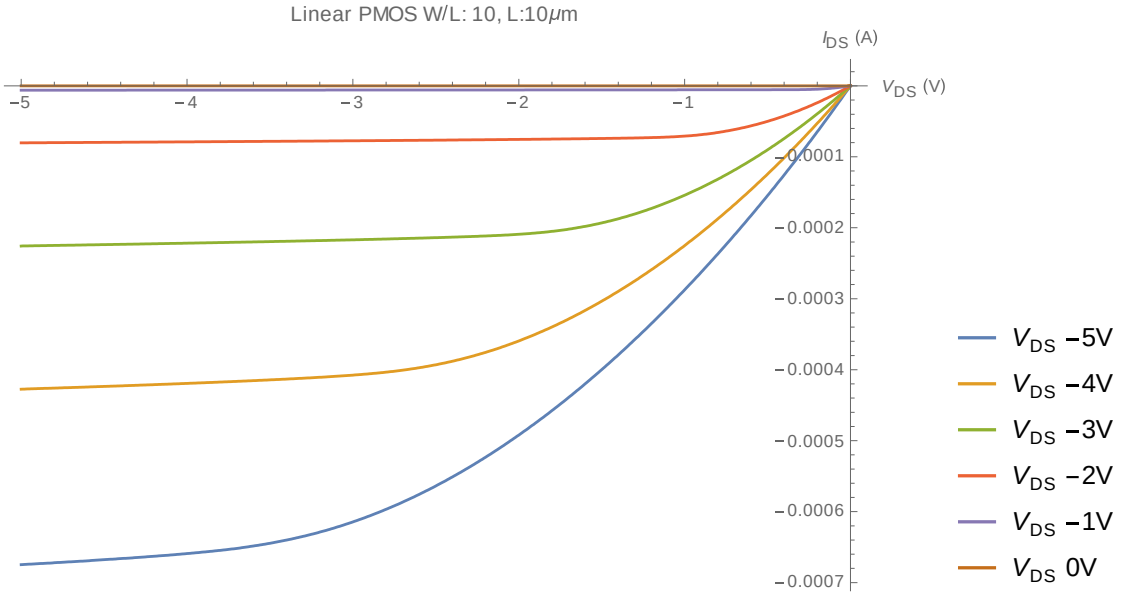

Figure 3.4.1: Linear PMOS $V_{DS}I_{DS}$

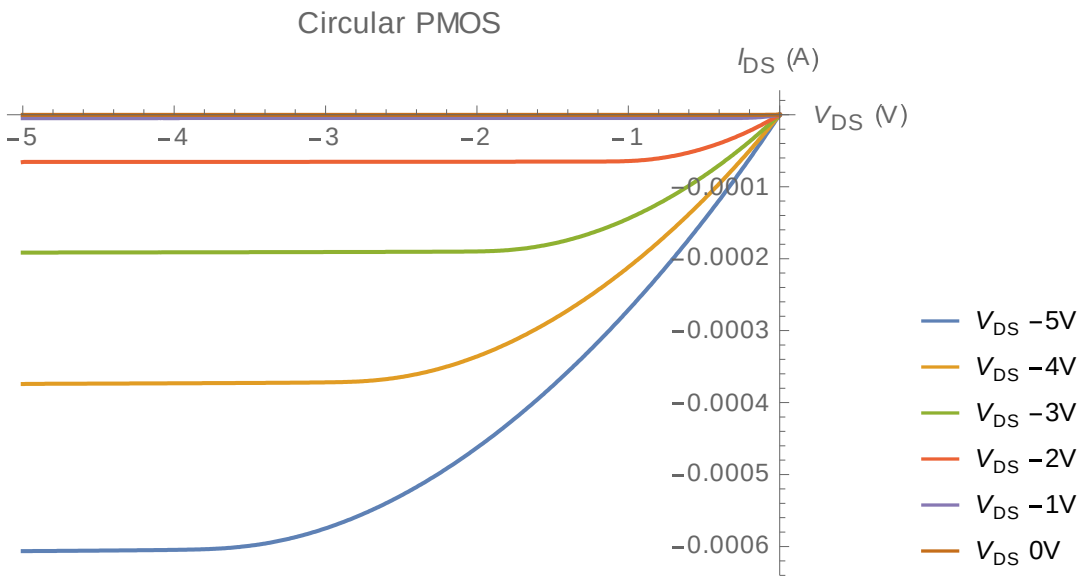

Figure 3.4.2 Circular PMOS $V_{DS}I_{DS}$

3.4.1 Parallel Resistance

In the below image we see that the resistance in the PMOS does not appear to be linear when the device should theoretically be off. However, a quick look at the current in this state gives the explanation: there is an offset current of around -10^{-8}A. This means that once it reaches its linear region, the resistance of 330MΩ is correct and high enough to not need to worry about

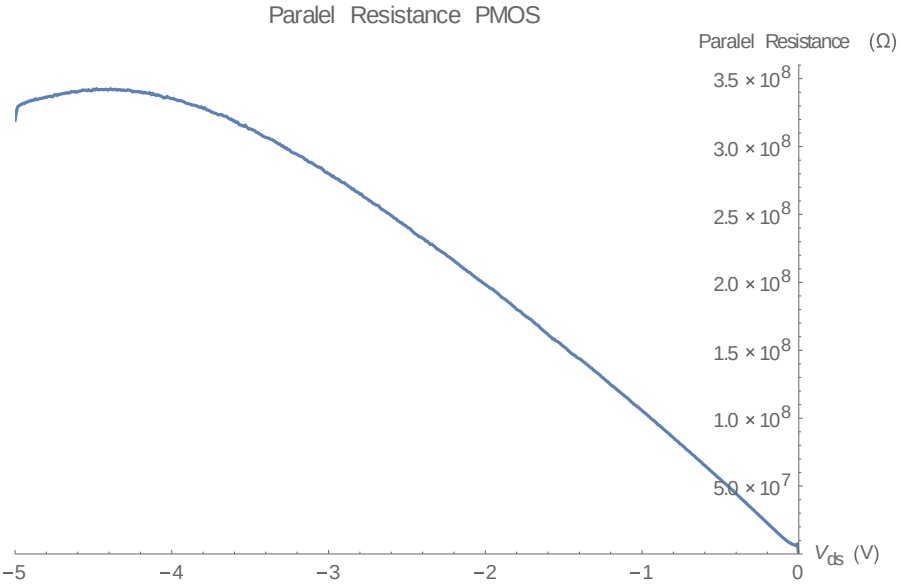

Figure 3.4.3 Parallel resistance in PMOS

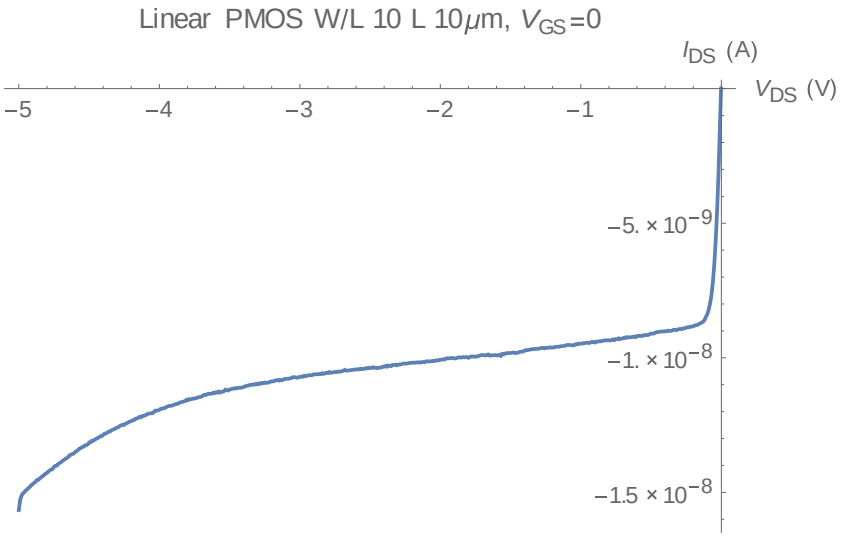

Figure 3.4.4 Expanded Linear MOS W/L 10 L 10µm V_{DS}=0

3.4.2 Channel Length Modulation

As we had less ability to test this wafer, we only have two data points on the curve. The same fitting formula was applied due to its high fitting level for the previous set. The r^2 value is not particularly valid due to the ability to always draw a line between two points. Unlike in the NMOS, the two W/L ratios agree on the λ values at their given points. The equation used to fit is $\lambda=0.032-0.0035\sqrt{L}$ V^{-1}. These tests were done on V_{GS}=-4V.

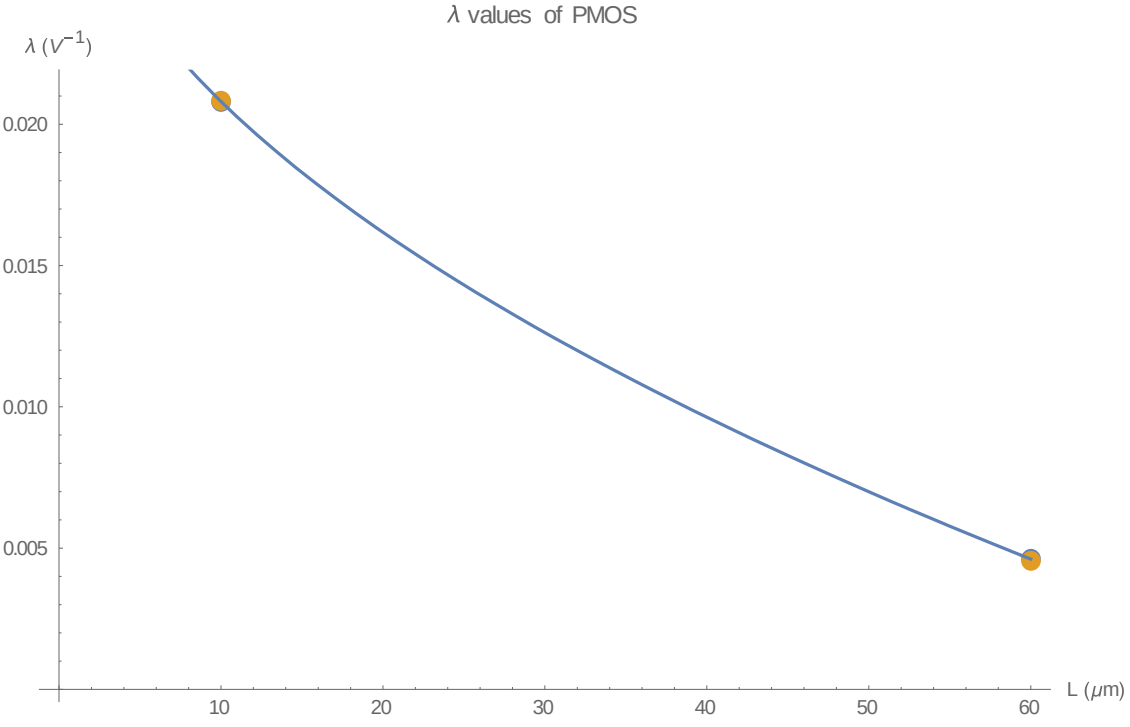

Figure 3.4.5 λ values of PMOS

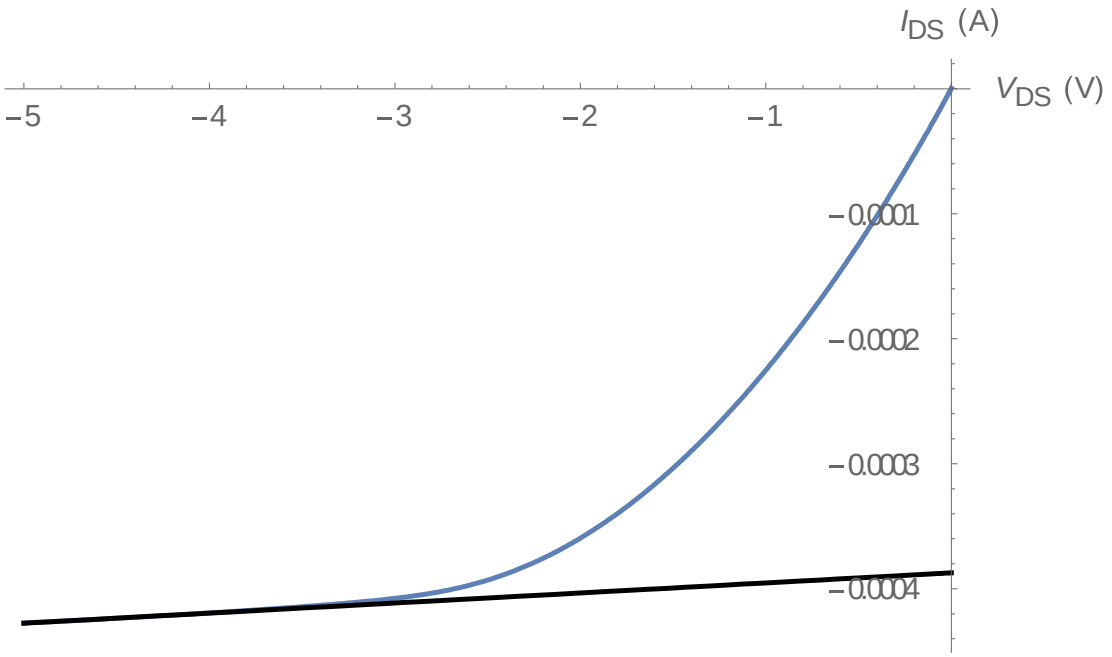

Figure 3.4.6: λ slope on W/L 10 L10µm PMOS

3.4.3 V_T Extraction

Extraction was done solely with the ELR method for PMOS, due to it being slightly more reliable when testing with the NMOS than the SD method. This is despite the fact that ELR would have more problems on NMOS than PMOS due to the parallel resistance. The threshold voltage for the PMOS is -0.656±0.016V.

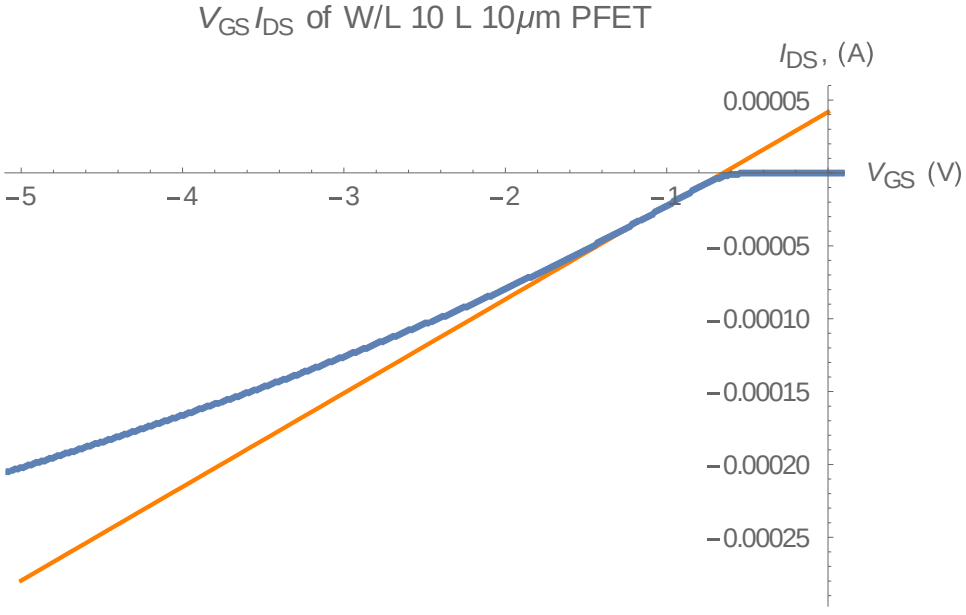

Figure 3.4.7 ELR extraction on PMOS

3.4.4 μ_p and C_{ox}

These were extracted in the same way as in NMOS. The result was $3.20*10^{-6}\frac{F}{Vs}$. As expected, this value is substantially lower than the value in PMOS due to the fact that PMOS devices universally have lower mobility than NMOS.

3.4.5 Table of Extracted Values

Table 3.4.1: PMOS Extracted Values

Parameter	Value or Equation
Parallel Resistance	330±2 MΩ
λ	$0.032 - 0.0035\sqrt{L}$ V^{-1}
V_T	0.656±0.016V
$\mu_p C_{ox}$	$6.40\pm0.037*10^{-6}\frac{F}{Vs}$
μ_p	202 cm^2/Vs

3.5 Device Modeling

Using the data gathered in the previous section, we can create a mathematical model of the MOSFET. The schematic used for simulation will be in the layout shown in figure 3.4.1 below. Both simulations (black lines show simulation) are quite close to the actual results. This verifies the analysis done in other sections, and means that the devices are reasonably close to the ideal and do not need to be analyzed using other models such as bulk charge theory [10]. The mathematical model is in Mathematica code as:

$$\text{iFET}[\text{vdi\_}, \text{vg\_}, \text{w\_}, \text{l\_}, \text{rs\_}, \text{rp\_}, \text{uc\_}, \text{vt\_}, \text{lam\_}] := (\text{vd}$$

$$= \text{vdi} - (\text{vdi}/\text{rp} + \text{uc} * \frac{w}{l} * \text{Piecewise}[\{\{(\text{vg} - \text{vt})\text{vdi} - \frac{\text{vdi}^2}{2}, \text{vdi}$$

$$\geq (\text{vg} - \text{vt})\}\}, \frac{(\text{vg} - \text{vt})^2}{2} * (1 + \text{lam} * (\text{vdi} - (\text{vg} - \text{vt})))]) * \text{rs};$$

$$\text{vd}/\text{rp} + \text{uc} * \frac{w}{l} * \text{Piecewise}[\{\{(\text{vg} - \text{vt})\text{vd} - \frac{\text{vd}^2}{2}, \text{vd} <$$

$$= (\text{vg} - \text{vt})\}\}, \frac{(\text{vg} - \text{vt})\text{^}2}{2} * (1 + \text{lam} * (\text{vd} - (\text{vg} - \text{vt})))])$$

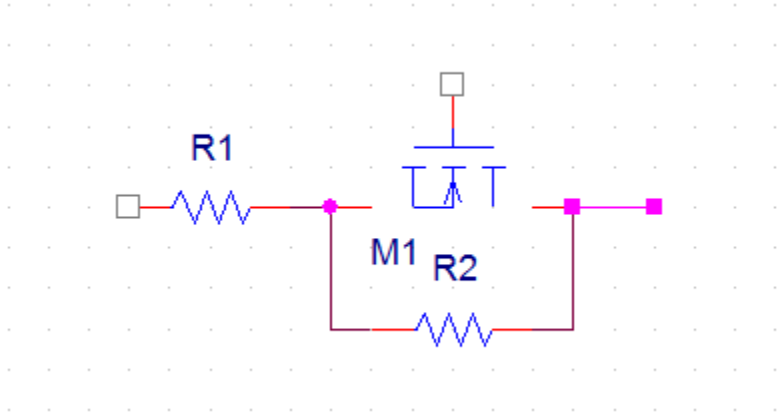

Figure 3.5.1 Model Effective Circuit

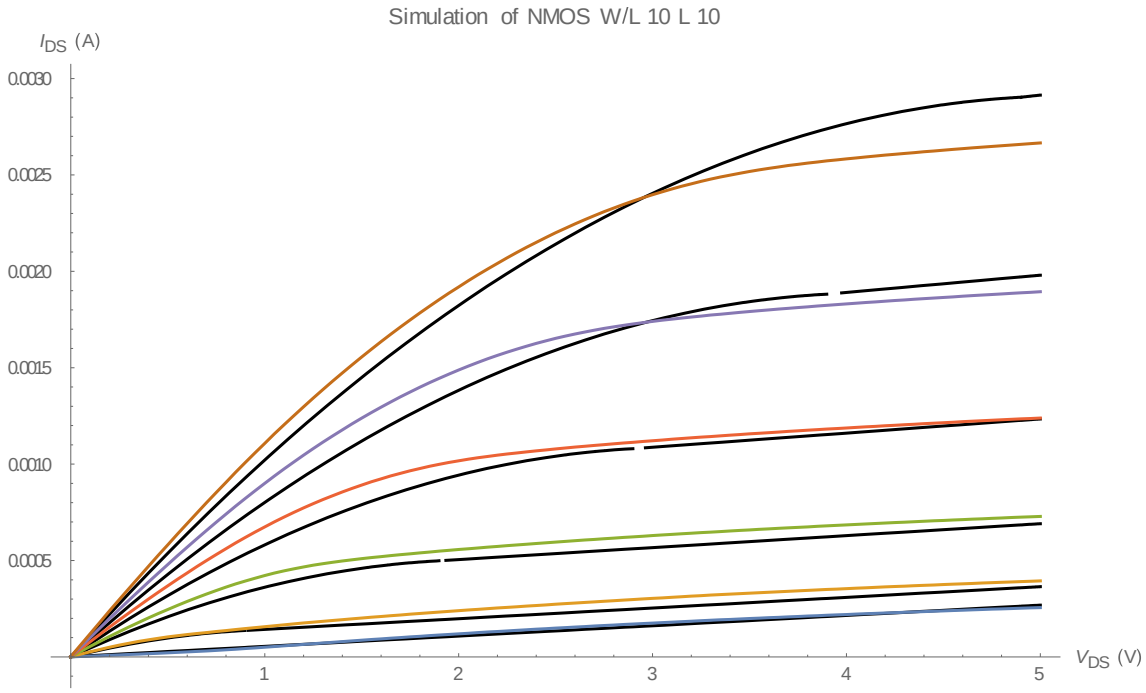

Figure 3.5.2 Simulation of NMOS comparison

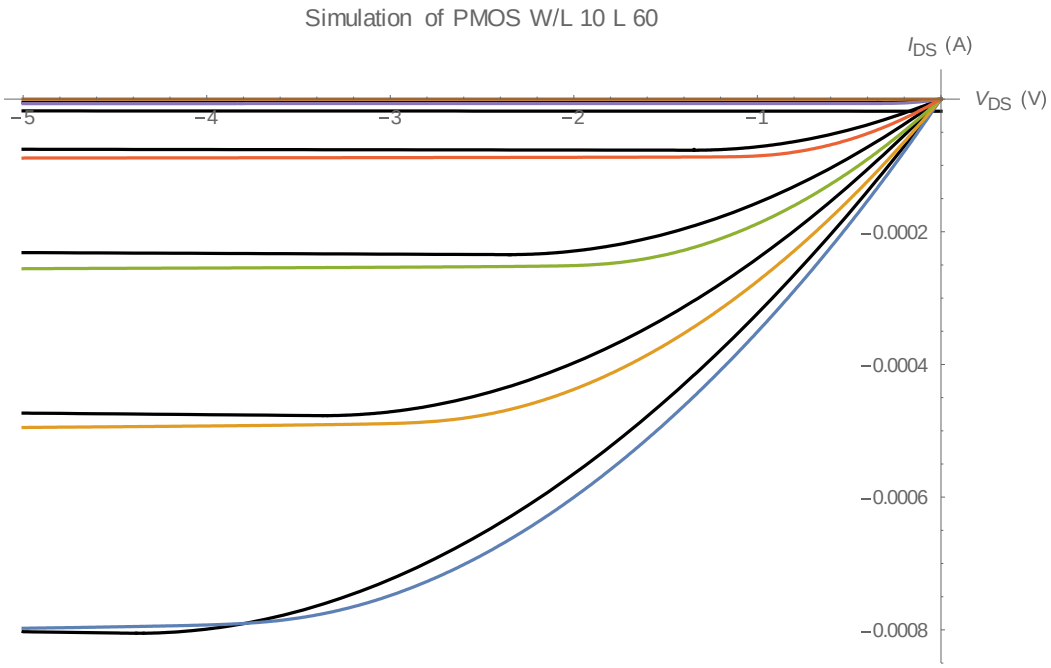

Figure 3.5.3 Simulation of PMOS comparison

3.6 Transconductance

Transconductance can be defined as the variation in drain current in response to corresponding gate voltage changes. This can be written as:

$$g_m = \frac{dI_D}{dV_{GS}}$$

where gm is the transconductance, Id is the drain current and VGS is the potential difference between the gate and the source. This is a very important parameter in determining the stability of the device, because we want to make sure a small change in gate voltage doesn't react uncontrollably by producing too much drain current response. This is also important if the devices are to be used as amplifiers, as it gives a glimpse into the amplification prowess of this device.

Threshold voltage (Vth) can also be extracted from the transconductance plots of MOSFETs. By using the transconductance change method, the Vth is the voltage at which the derivative of the low drain voltage gm dgm/dVgs is maximum. This doesn't take into account electron mobility degradation and the effect of series resistance.

Below are graphs showing the transconductance of our nMOS devices.

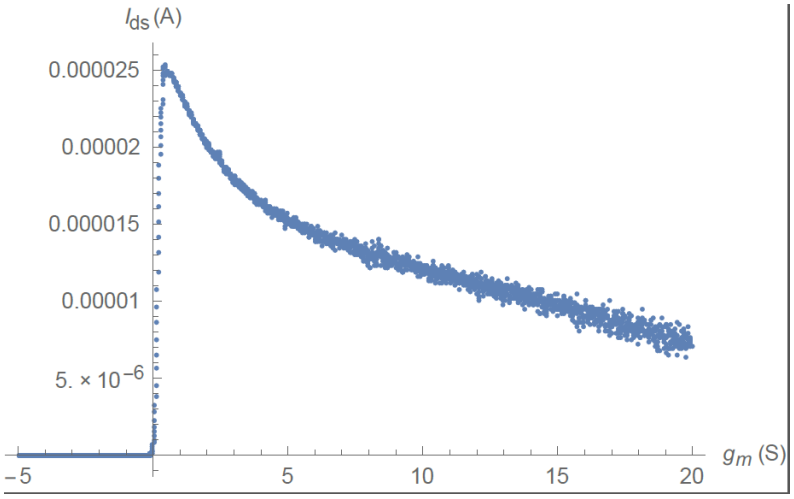

Figure 3.6.1 Transconductance vs Ids for linear nMOS of W/L ratio 10

3.7 Capacitance-Voltage Measurements

Each die was fabricated with three MOS capacitors in order to facilitate capacitance-voltage measurements. These devices were circular capacitors with a radius of 400 um. When taking measurements one probe was put in contact with the stage of the measurement device, thus making indirect contact with the substrate of the wafer. The other probe was placed in contact with the metal top plate of the capacitor. Capacitance was recorded across a DC voltage sweep with a small AC voltage signal at a constant frequency. This was done for a range of frequencies for each device measured.

These measurements were done as the data can be used to calculate several properties of the devices fabricated. It is possible to extract the oxide capacitance, the oxide thickness, the fixed oxide charge, the flatband voltage, the threshold voltage, and the maximum depletion width.

3.7.1 PMOS

The Capacitance-Voltage (C-V) measurements were done to obtain C-V characteristics at high and low frequencies and determine important MOS parameters such as oxide thickness (t_{ox}), Depletion capacitance, maximum depletion width, oxide fixed charges etc. For our measurements all the Group-2 n-type Si wafers (PMOS) wafers were discarded as it was discovered that the nitride layer was left un-etched. So we had to borrow n-type Wafer -3 from group -3 for all our PMOS characterization purpose. This analysis is shown for two different dies on the same wafer.

There are 3 important parameters that can be calculated from the obtained C~V characteristics-

- Oxide capacitance (C_{ox})
- Oxide thickness (t_{ox})
- Fixed oxide charge (Q_F)

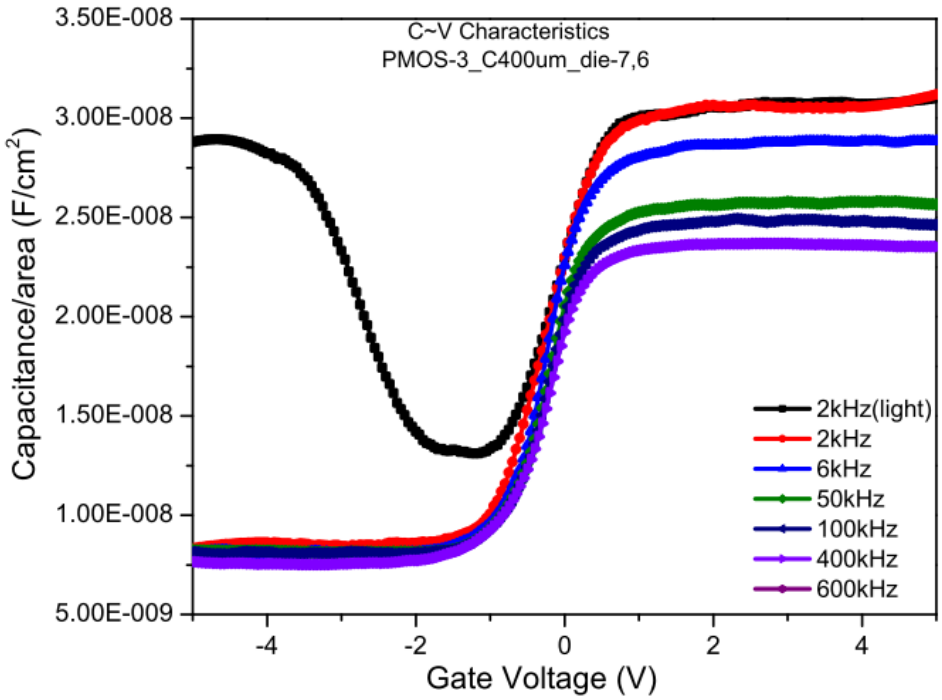

Figure 3.7.1. C-V characteristics of 400µm radius PMOS capacitor on Wafer-3, die - (7, 6).

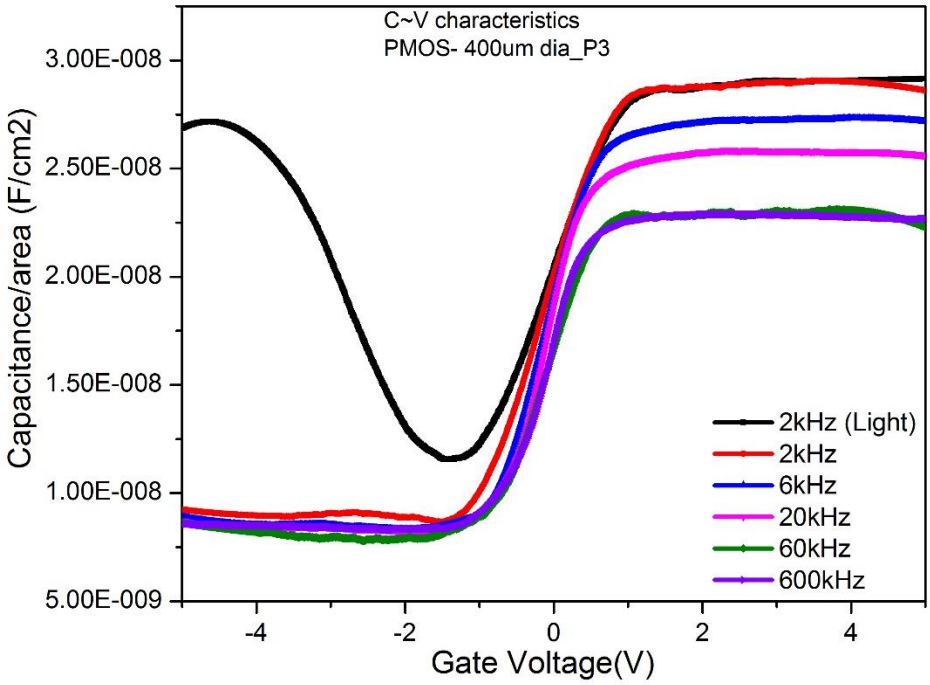

Figure 3.7.2. C-V characteristics of 400µm radius PMOS capacitor on Wafer-3, die - (3, 4).

From the C-V characteristics shown in figure, we can see at low frequency (2 kHz), there are not enough minority charge carriers in dark to produce an ideal low frequency characteristics. But when light was shined on top of the wafer, the C-V showed a close to ideal response due to extra photo-generated minority carrier generation.

The accumulation region for PMOS capacitors lie on the right hand side of the C-V curves. The accumulation capacitance is approximated to be the oxide capacitance. The capacitor area was calculated by using its radius as 400µm to be $A = \pi*(400\mu m)^2 = 5.03 \times 10^{-3}$ cm^2. The determined oxide capacitance can be used to calculate the oxide thickness by using the formula-

$$C_{OX} = \frac{\varepsilon_{OX}\varepsilon_0 A}{t_{OX}}$$

The calculated oxide capacitance and oxide thickness for the two PMOS capacitors are tabulated below.

Table 3.7.1. Oxide capacitance and oxide thickness for different PMOS capacitors

Wafer No. (Die No.)	Oxide Capacitance, C_{ox} (pF)	Oxide Thickness, t_{ox} (nm)
Wafer-3 (7, 6)	155	112
Wafer-3 (3, 4)	146	118

The calculated value of oxide thickness is found to be in close agreement with the oxide thickness of ~100nm. Also the oxide capacitance was found to be close to the calculated value of ~173pF for a capacitor with 100nm oxide thickness and 400 μm radius. The deviation can be attributed to the uneven thickness of oxide over the wafer.

Next, the Depletion capacitance and maximum depletion width can be determined by, taking the minimum capacitance in the high frequency C-V characteristics. This total capacitance is the series combination of minimum depletion capacitance and the oxide capacitance. Hence depletion capacitance can be calculated by-

$$C = \frac{C_{ox}C_{dep}}{C_{ox} + C_{dep}}$$

Thus,

$$C_{dep} = \frac{C_{ox}C}{C_{ox} - C}$$

The calculated Depletion capacitance and maximum depletion width are tabulated below.

Table 3.7.2. Observed Total capacitance, Depletion capacitance and maximum depletion widths.

Wafer No. (Die No.)	Total Capacitance, C (pF)	Depletion Capacitance, C_{ox} (pF)	Maximum Depletion Width, W_{max} (μm)
Wafer-3 (7, 6)	38.0	50.3	1.03
Wafer-3 (3, 4)	42.6	60.1	0.86

The acceptor doping density can be determined from the C-V characteristics by plotting ($1/C^2$) vs. V_G and calculating the doping concentration from the slope of high frequency curve in depletion region by the formula-

$$N_D = \frac{2}{q\varepsilon_0\varepsilon_s A^2 \left|\frac{d}{dV}\left(\frac{1}{C^2}\right)\right|}$$

Where, the derivative term in the denominator is the slope of high frequency curve in depletion region. The calculated acceptor doping densities along with observed threshold voltages is given below-

Table 3.7.3. Acceptor doping density and threshold voltages for different PMOS capacitors.

Wafer No. (Die No.)	Acceptor doping density, N_A (cm^{-3})	Threshold Voltage, V_{th} (V)
Wafer-3 (7, 6)	1.23×10^{15}	-1.6

Wafer-3 (3, 4)	1.33 x 10^{15}	-1.3

As seen from the table, the acceptor doping concentrations and threshold voltage values are very close to each other. The threshold voltage values are negative indicating that the PMOS devices are Enhancement type and the channel formation takes place in inversion regime.

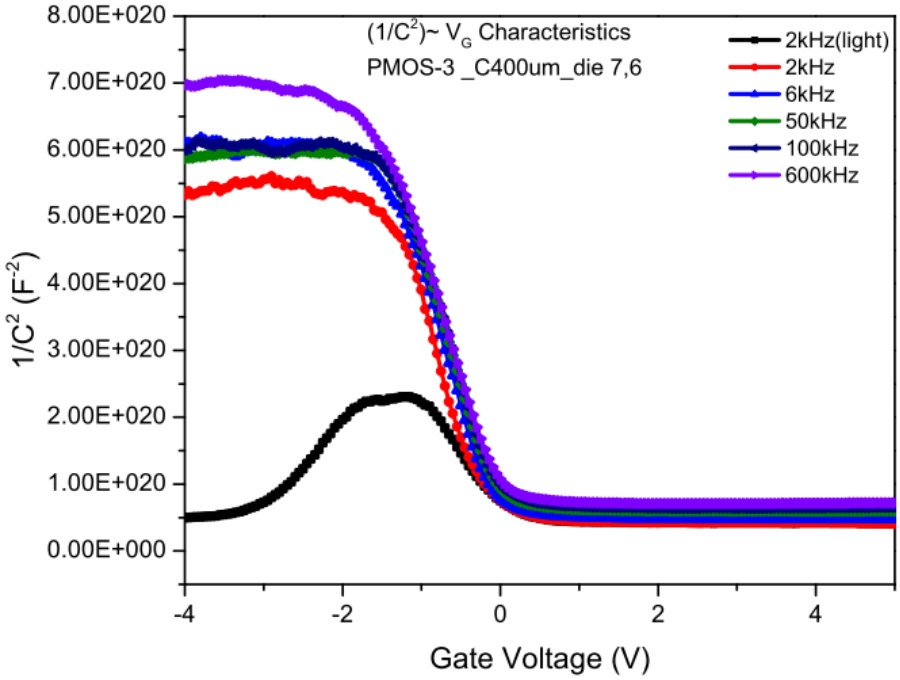

Figure 3.7.3. $(1/C)^2$ ~ V_G characteristics of 400µm radius PMOS capacitor on Wafer-3, die - (7, 6).

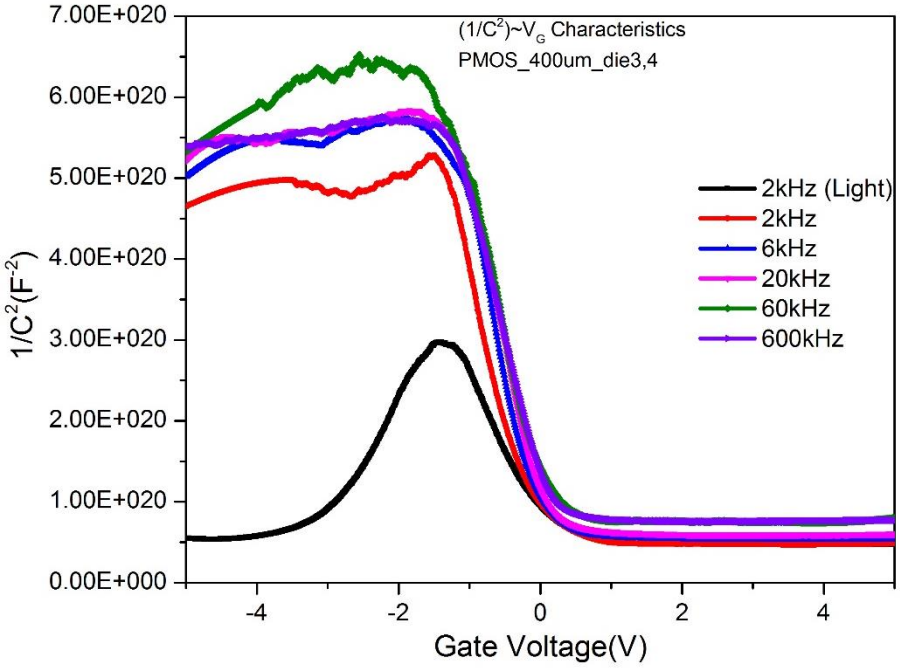

Figure 3.7.4. $(1/C)^2$ ~ V_G characteristics of 400µm radius PMOS capacitor on Wafer-3, die - (3, 4)

Finally, the oxide fixed charge density as an important parameter in MOS characterization must be determined in order to control threshold voltage shift. The Flat band voltage of a MOS capacitor is given by,

$$V_{FB} = \varphi_{ms} - \frac{Q_F}{C_{ox}}$$

Where, V_{FB} is the flat band voltage, φ_{ms} is the work function difference between metal and semiconductor, C_{ox} is the oxide capacitance and Q_F is the fixed oxide charge.

From the above relation we can observe that the variation in flat band voltage from ideal value to observed value is due to the fixed oxide charge. Hence change in flat band voltage between simulated C-V characteristic and measured C-V characteristic, must give us the fixed oxide charge using the above mentioned equation. The simulated C-V characteristics of the PMOS capacitor is shown in Figure below.

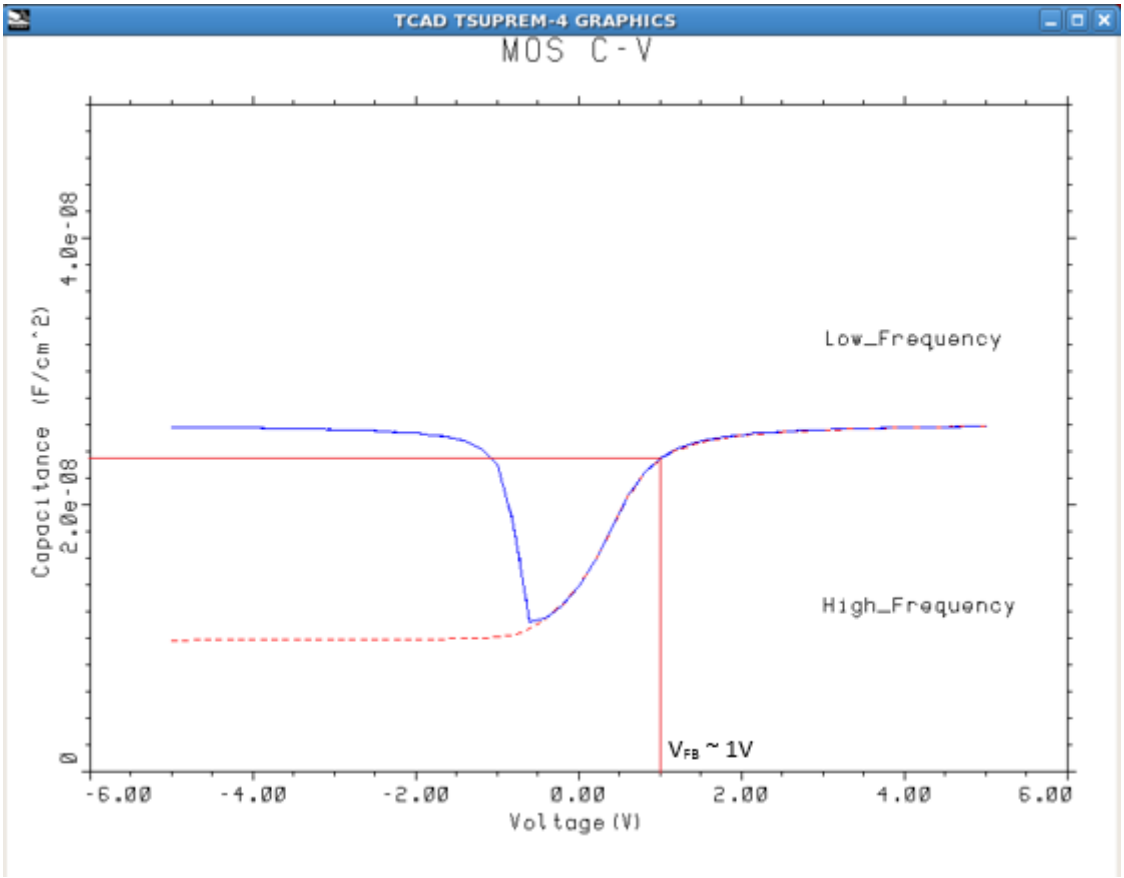

Figure 3.7.5. Simulated C~V characteristic of PMOS capacitor by TSUPREM-4 with V_{FB} ~ 1V.

The flat band capacitance is assumed to be 90% of the oxide capacitance and the corresponding flat band voltage from the simulated curve was determined to be about 1V. The shift in observed flat band voltage from simulated value was used to find the fixed oxide charge and is tabulated in the following table.

Table 3.7.4. Calculated Flat Band Voltage, Flat Band Voltage shift, Oxide capacitance and Fixed oxide charges for different PMOS capacitors.

Wafer No. (Die No.)	Flat Band Voltage, V_{FB} (V)	Flat Band Voltage Shift, ΔV_{FB} (V)	Oxide Capacitance, C_{ox} (pF)	Fixed Oxide Charge, Q_F (C/m^2)	Fixed Oxide Charge, Q_F (e/m^2)
Wafer-3 (7, 6)	0.36	-0.64	155	9.9×10^{-11}	6.2×10^{-8}
Wafer-3 (3, 4)	0.57	-0.43	146	7.7×10^{-11}	4.8×10^{-8}

The fixed oxide charge doesn't cause a change in shape of the C-V characteristics, but merely shifts the PMOS curves. The obtained value of fixed oxide charges along with flat band voltage shift can be used to produce a model which can closely approximate the real device.

3.7.2 NMOS

In the accumulation region, the far negative region of the voltage sweep for an NMOS capacitor, the total capacitance of the device is the capacitance of the oxide. Using the equation for a parallel plate capacitor with a dielectric medium the oxide thickness can be calculated.

$$C_{ox} = \frac{\varepsilon_{ox}\varepsilon_0 A}{t_{ox}}$$

Rearranging the equation algebraically gives

$$t_{ox} = \frac{\varepsilon_{ox}\varepsilon_0 A}{C_{ox}}$$

The capacitor has an area of $5.027 * 10^{-7}$ m^2, and ε_{ox} is taken to be 3.9. The calculated thickness of the oxide layer for several devices are shown in the following table.

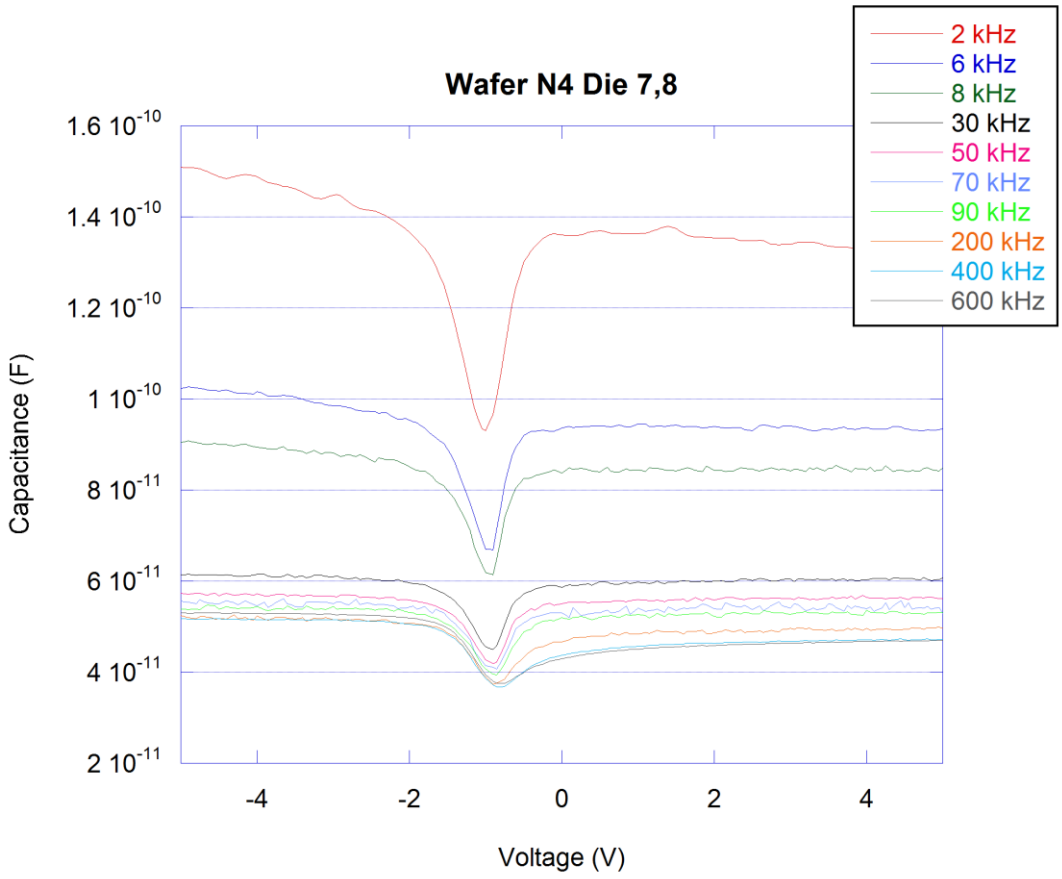

Figure 3.7.1 CV Wafer N4 Die 7,8

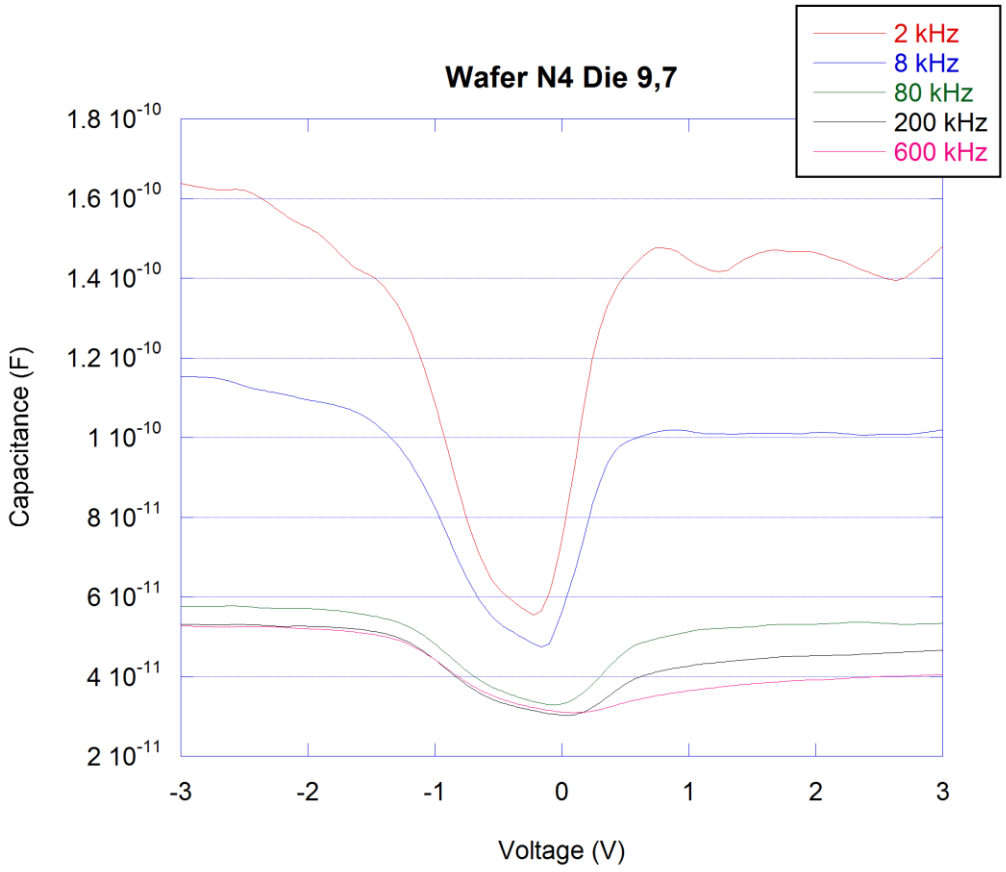

Figure 3.7.2 CV Wafer N4 Die 9,7

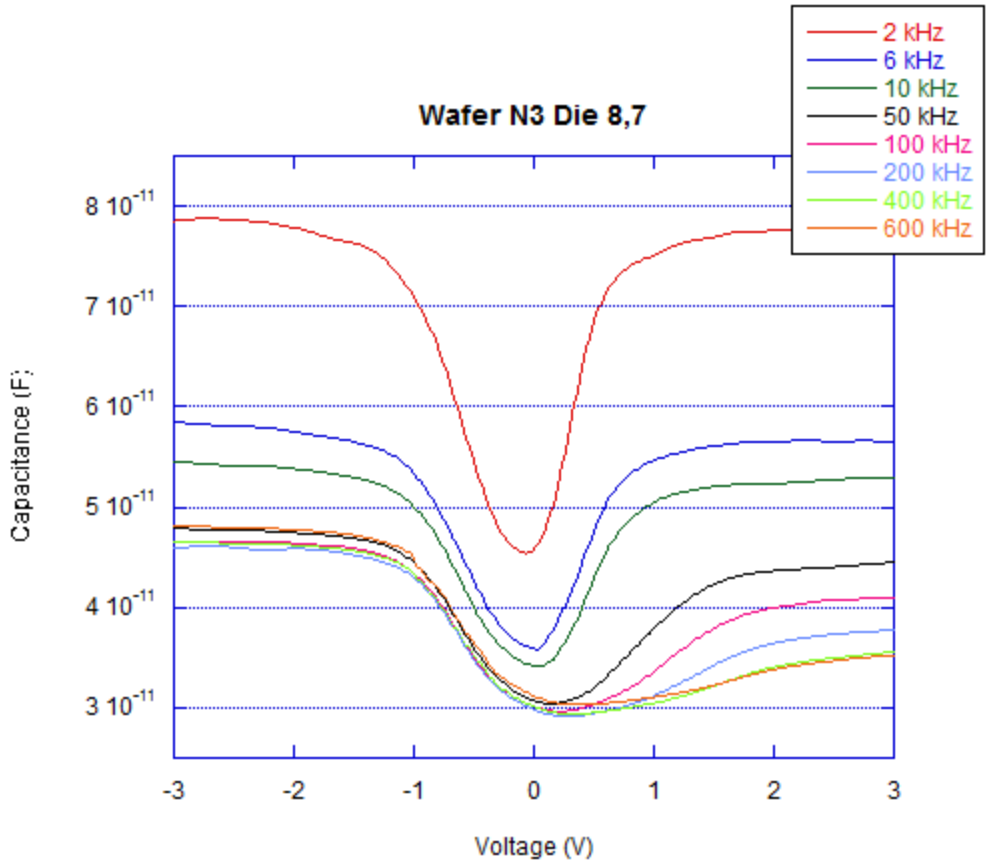

Figure 3.7.3 CV Wafer N3 Die 8,7

Die	C_{ox} (pF)	T_{ox} (nm)
Wafer N4 Die 7,8	150	116
Wafer N4 Die 9,7	160	106
Wafer N3 Die 8,7	79	220

Table 3.7.1 Oxide Thickness

The depletion width can be determined from a high frequency C-V curve. At the beginning of the inversion region the capacitance due to the depletion region, and thus the depletion width, are at a maximum. At this point the total capacitance is due to the capacitance of the oxide and the depletion region. The total capacitance is expressed by following equation.

$$\frac{1}{C_{total}} = \frac{1}{C_{ox}} + \frac{1}{C_{DL}} \text{ or } C_{total} = \frac{C_{ox}C_{DL}}{C_{ox}+C_{DL}}$$

The capacitance of the depletion region can be modeled as a parallel plate capacitor.

$$C_{DL} = \frac{\varepsilon_{Si}\varepsilon_0 A}{W_{max}}$$

Rearranging this equation algebraically gives

$$W_{max} = \frac{\varepsilon_{Si}\varepsilon_0 A}{C_{DL}}$$

The high frequency CV data shown does not show the expected behavior of a high frequency signal. The capacitance increases past the threshold voltage, instead of remaining constant. This indicates that there is an inversion layer, which affects the total capacitance. This means that the total capacitance used to calculate the maximum depletion width will be higher than the actual value, and the calculated depletion width will be less than actual. The calculated depletion widths are shown in the table below.

Die	C_{dep} (pF)	W (μm)
Wafer N4 Die 7,8	50	1.04
Wafer N4 Die 9,7	38	1.36
Wafer N3 Die 8,7	49	1.05

Table 3.7.2 Depletion Width

Higher frequency data, which theoretically would have given better results for the depletion width, was not taken as the data started to show irregular behavior at higher frequencies. This irregular behavior was seen across multiple wafers, both NMOS and PMOS, and was thus assumed to be due to the measurement method rather than the device being measured.

The threshold voltage can be determined by finding the point at which the derivative of the capacitance goes to zero. The threshold voltage was found for several dies, and they are listed in the table below.

Die	V_T
Wafer N4 Die 7,8	-0.75
Wafer N4 Die 9,7	0.1

Wafer N3 Die 8,7	0.36

Table 3.7.3 Threshold Voltage

It is possible to determine the doping density of the channel by plotting the inverse of the capacitance squared against the applied voltage. The slope of this plot in the depletion region can then be used to calculate the dopant concentration. The dopant concentration can be calculated using the equation:

$$N_D = \frac{2}{qA^2 \left| \frac{d(1/C^2)}{dV} \right|}$$

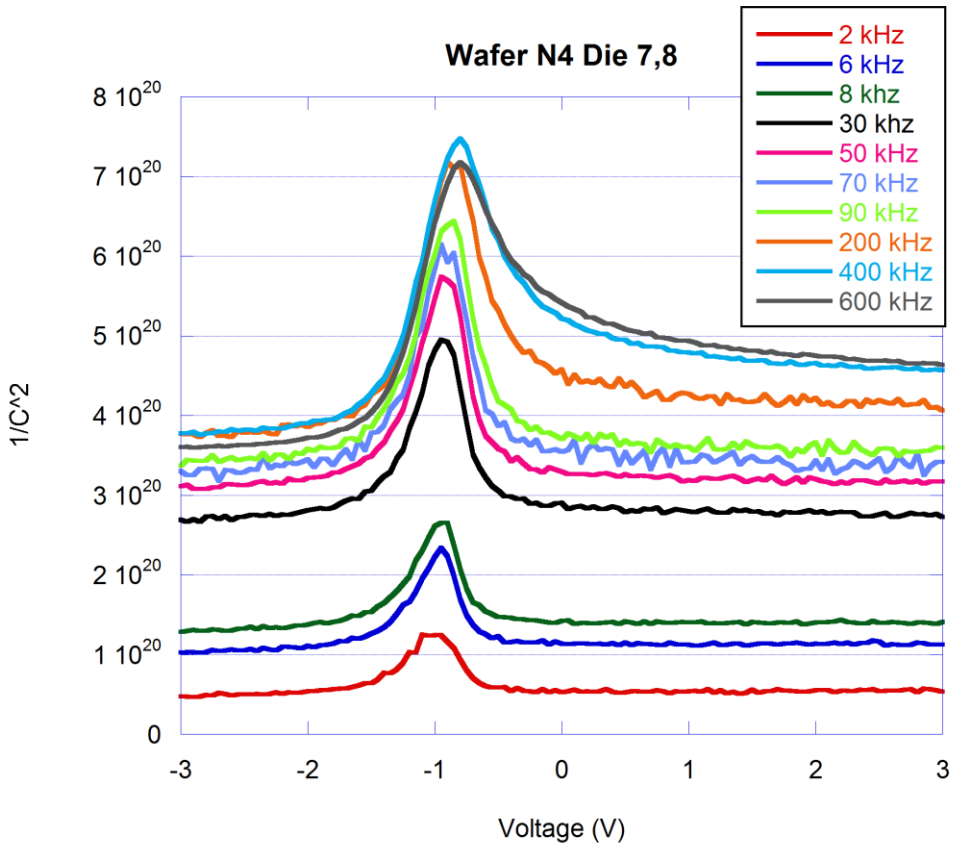

Figure 3.7.4 $1/C^2$ Wafer N4 Die 7,8

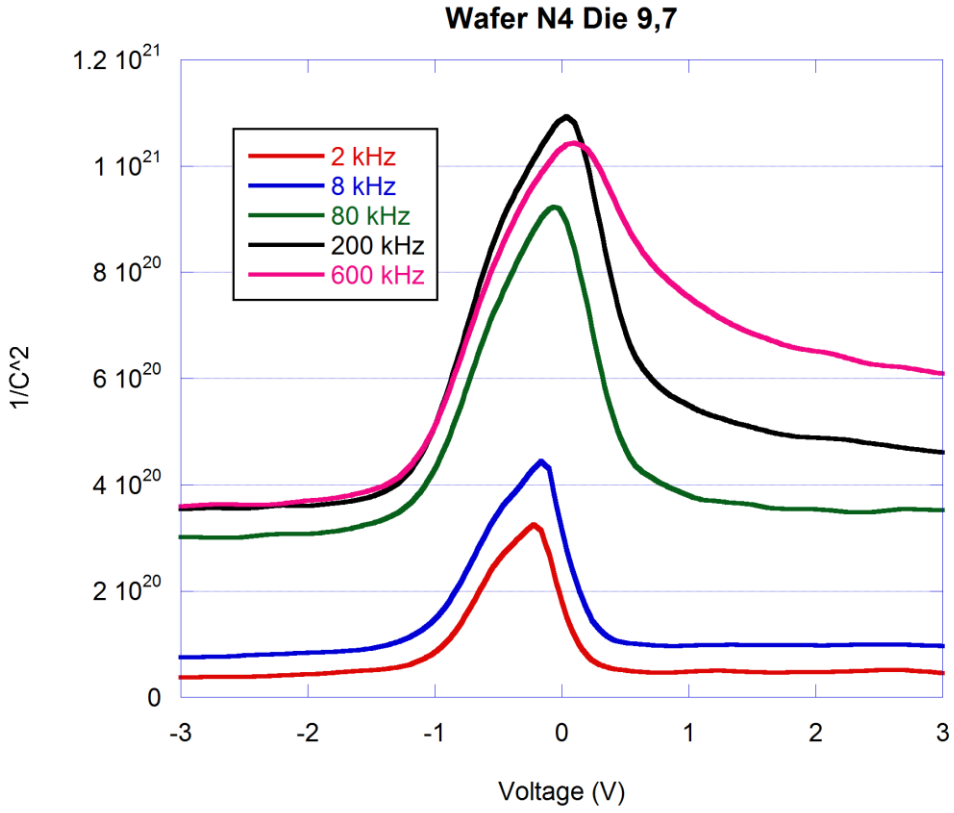

Figure 3.7.5 $1/C^2$ Wafer N4 Die 9,7

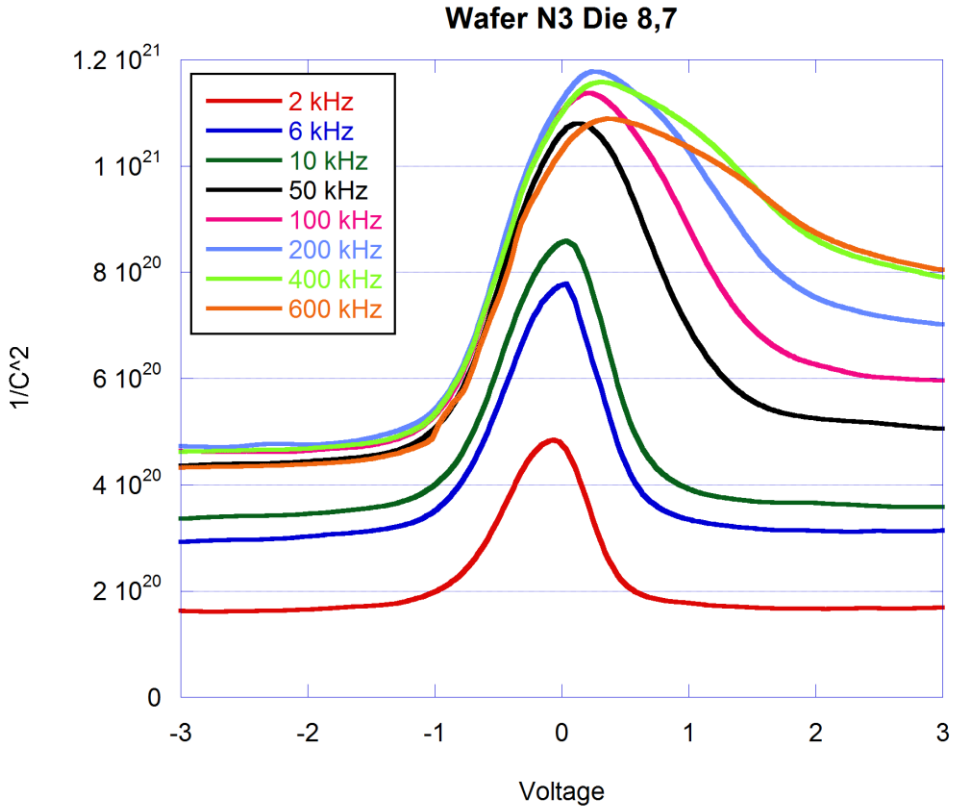

Figure 3.7.6 $1/C^2$ Wafer N3 Die 8,7

The dopant concentration was found for several die. These values are shown in the following table.

Table 3.7.4 Dopant Concentration

Die	$d(1/C^2)/dV$ ($F^{-2}V^{-1}$)	N_D (cm^{-3})
Wafer N4 Die 7,8	$4.4*10^{20}$	$1.1*10^{17}$
Wafer N4 Die 9,7	$5.6*10^{20}$	$8.8*10^{16}$
Wafer N3 Die 8,7	$6.2*10^{20}$	$7.9*10^{16}$

It is possible to estimate the fixed oxide charge from the capacitance-voltage curve. This is done by comparing the measured flatband voltage to the flatband voltage based on simulation. The simulation does not simulate the generation of fixed oxide charge, this means that the change in the flatband voltage compared to the simulation is due to the fixed oxide charge in the device. For the purposes of comparison the flatband voltage was assumed to be the voltage at which the capacitance became ninety percent of the oxide capacitance.

The flatband voltage is related to the fixed oxide charge by the equation:

$$Q_f = \frac{-\Delta V_{FB} C_{ox}}{A}$$

Table 3.7.5 Fixed Oxide Charge

Die	ΔV_{FB}	C_{ox} (pF)	Q_f (mC/m^2)
Wafer N4 Die 7,8	-0.70	150	.209
Wafer N4 Die 9,7	-0.55	160	.175
Wafer N3 Die 8,7	0.16	79	-.025

3.8 Effect of Substrate Biasing

In the previous MOSFET characterizations, the substrate was grounded, so at V_{sub} = 0V, the threshold voltage is defined when the condition $\varphi_s = \varphi_f$ is satisfied. But when a positive voltage is applied to the substrate of a PMOSFET or a negative voltage is applied to NMOSFET, the threshold voltage shifts towards more negative and more positive respectively. This threshold voltage shift can be expressed by the equation:

$$\Delta V_{th} = \frac{\sqrt{2q\varepsilon_s\varepsilon_0 N_A}}{C_{ox}}\left[\sqrt{2\varphi_f + V_B} - \sqrt{2\varphi_f}\right]$$

The graphs below show the transfer characteristics (I_D ~ V_G) of NMOSFET and PMOSFET under different substrate bias conditions. The NMOSFET was subjected to a substrate bias range of -10.5V to 0V and the PMOSFET was subjected to 0V to 10.5V. The transfer characteristics under different biases was then used to determine the threshold voltages at those bias voltages.

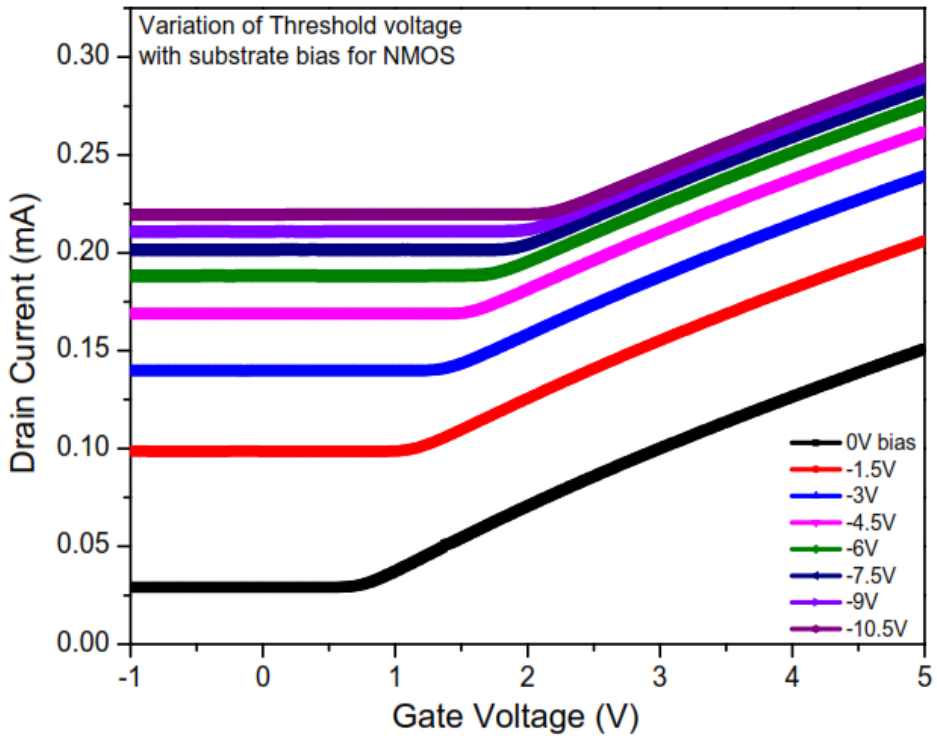

Figure 3.8.1 I_D ~ V_G Characteristics for a linear NMOSFET of 100µm length under various substrate bias voltages (0 to -10.5 V).

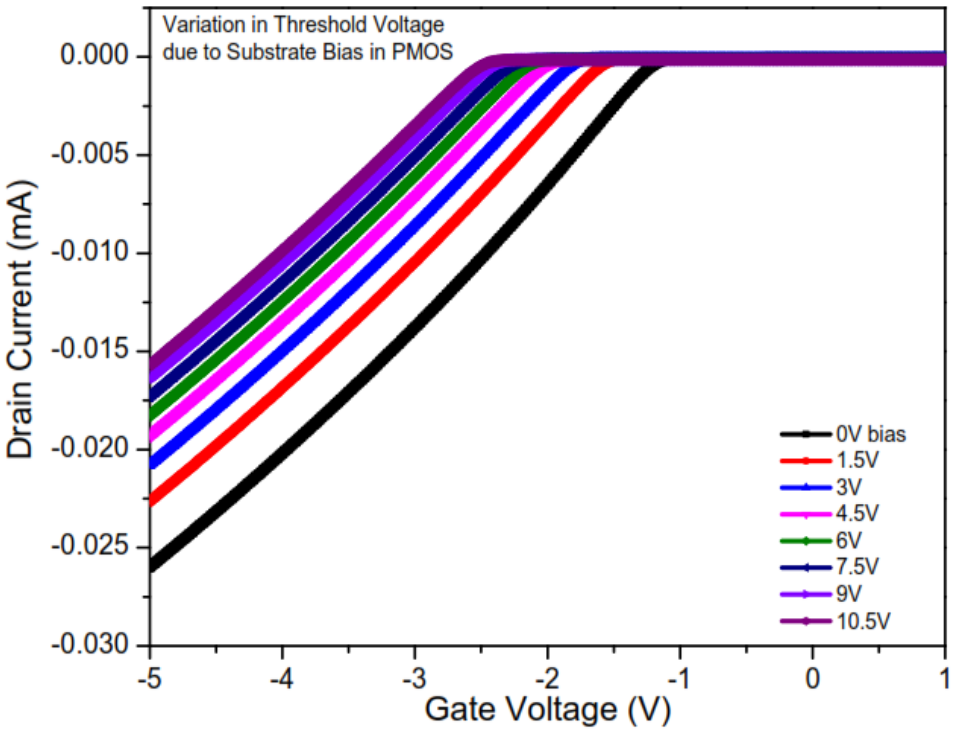

Figure 3.8.2 I_D ~ V_G Characteristics for a linear PMOSFET of 100µm length under various substrate bias voltages (0 to 10.5 V).

The threshold voltages were calculated from the I_D ~ V_G characteristics by transconductance method. First transconductance was calculated by taking derivative of I_D ~ V_G curves and then derivative of transconductance is taken and plotted against gate voltage. The peak of derivative of transconductance gives the threshold voltage. The threshold voltages for different substrate bias for NMOS and PMOS were calculated and plotted against the bias voltages. The plot is as shown in figures below. It can be observed from the plots that for both NMOS and PMOS, threshold voltage increases for increase in bias applied. For NMOS, with increasing negative bias on the gate, the threshold voltage increases almost linearly. Similarly for PMOS, with application of progressively higher gate voltage, the threshold voltage increases in negative direction. This is due to the fact that, due to increasing substrate bias, the potential of gate decreases and higher potential is required to attract the minority carriers to form the inversion layer.

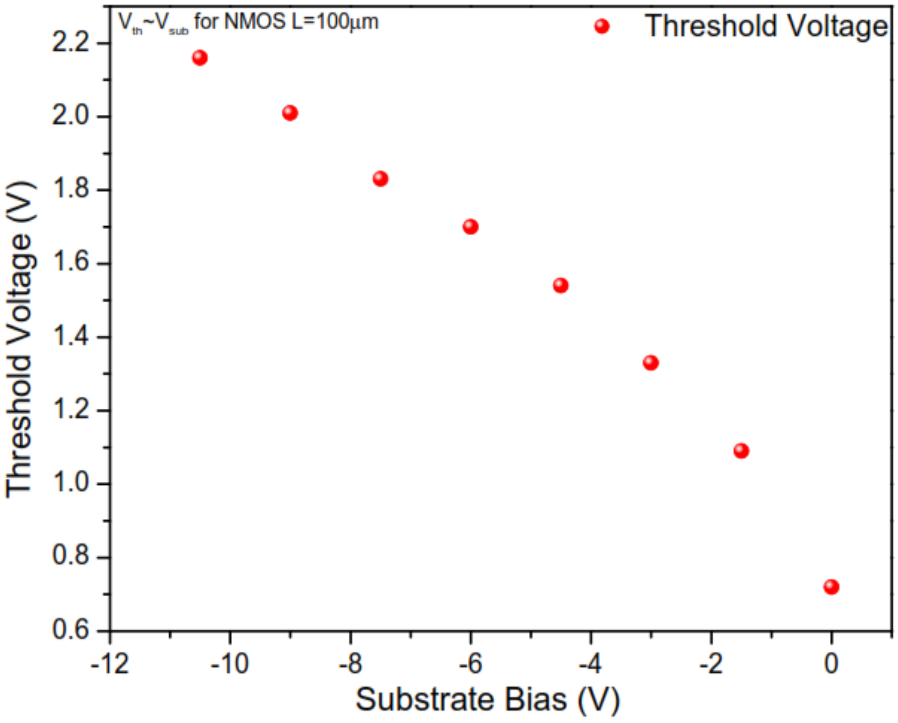

Figure 3.8.3 Threshold voltage as a function of substrate bias for linear NMOS of channel length L=100µm.

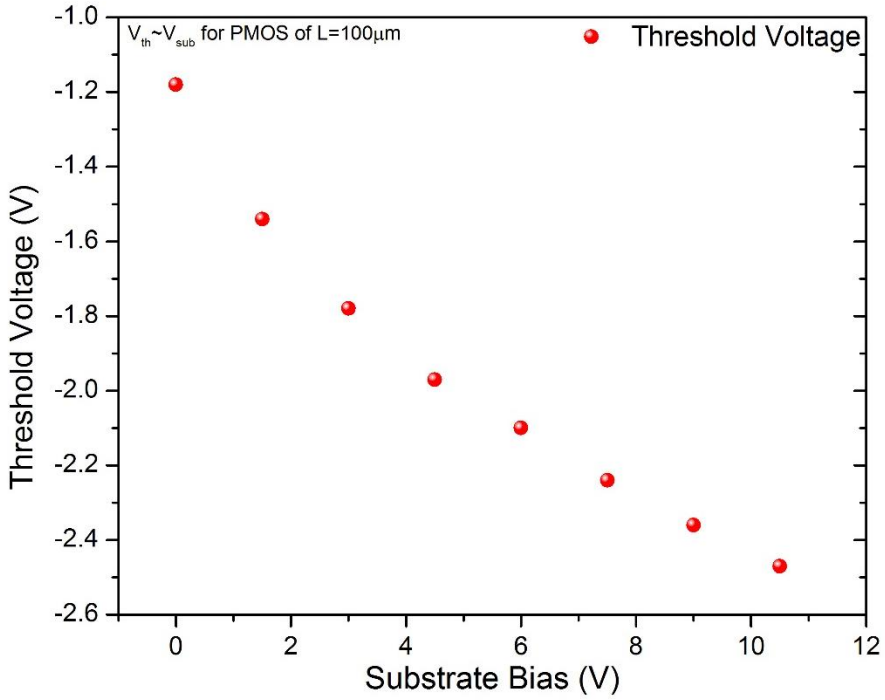

Figure 3.8.4 Threshold voltage as a function of substrate bias for linear PMOS of channel length L=100µm.

3.9 Subthreshold Voltage Swing

In ideal MOSFETs, at any gate voltage below or equal to threshold voltage, drain current is zero. But in real MOSFETs, the drain current increases with gate voltage below threshold voltage due to presence of weak inversion layer. This weak inversion layer causes a diffusion current to flow known as Sub-threshold current. It is given by:

Subthreshold Swing (ss) is defined as the amount of gate voltage change that causes the drain current to change by a decade. Hence it can be determined by the reciprocal of the slope of the log(I_{DS}) vs. V_{GS} curve in subthreshold region.

$$ss = \left(\frac{\partial log I_{DS}}{\partial V_{GS}}\right)^{-1} = ln10\frac{kT}{q}\left(1+\frac{C_{dep}}{C_{ox}}\right)$$

The ideal subthreshold swing for a MOSFET at room temperature is ~60mV/decade. Smaller the subthreshold swing, even a small change in gate voltage can produce significant change in drain current. So to determine the subthreshold swing for NMOS and PMOS, the transfer characteristics was plotted in semi-log scale as shown in figures. The subthreshold swing for circular NMOSFETs was found to vary between 188mV/decade to 195mV/decade for different channel lengths as shown in figure below.

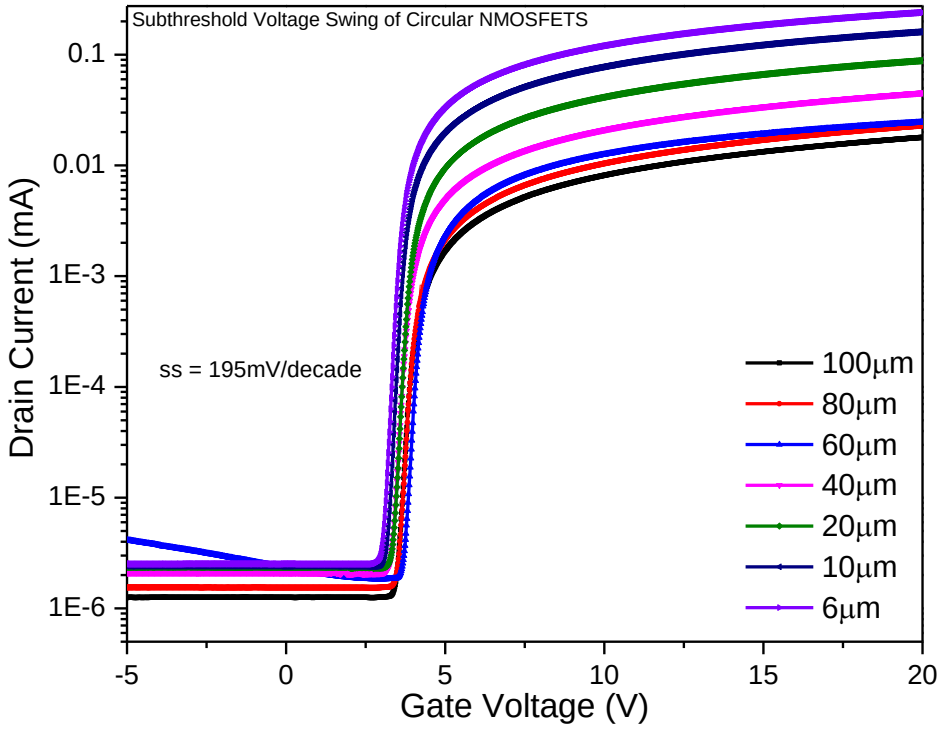

Figure 3.9.1 log (I_{DS})-V_{GS} characteristics to determine the sub-threshold voltage swing of circular NMOSFETs of different channel lengths.

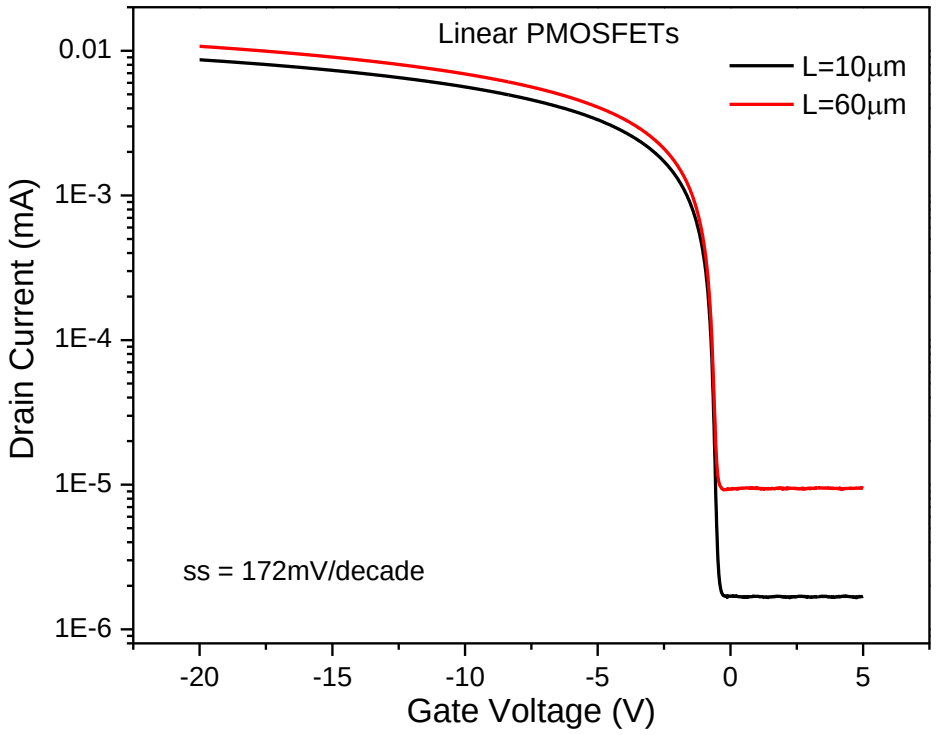

Figure 3.9.2 log (I_{DS})-V_{GS} characteristics to determine the sub-threshold voltage swing of linear PMOSFETs of different channel lengths.

The oxide and depletion capacitances can be determined by using the given formula above. The subthreshold swing was also calculated for linear PMOSFETs as shown in the figure above. The subthreshold voltage swing was found to be ~172mV/decade for the linear PMOSFETs for different channel lengths. The ss values were found to be almost same for different sizes of p- and n-MOSFETs.

3.10 On State Resistance

Drain current in linear region is given by,

$$I_D = \frac{\mu_P Z C_i}{L}\left[(V_G - V_T)V_D - \frac{{V_D}^2}{2}\right]$$

The slope of the I_D vs. V_D curve changes in linear region, depending on the channel length with gate voltage kept constant as can be seen from the equation above. In the figure below, the output characteristics of various circular NMOS transistors in linear region ($0.1V <= V_{DS} <= 0.5V$) at constant gate voltage of 5V has been plotted.

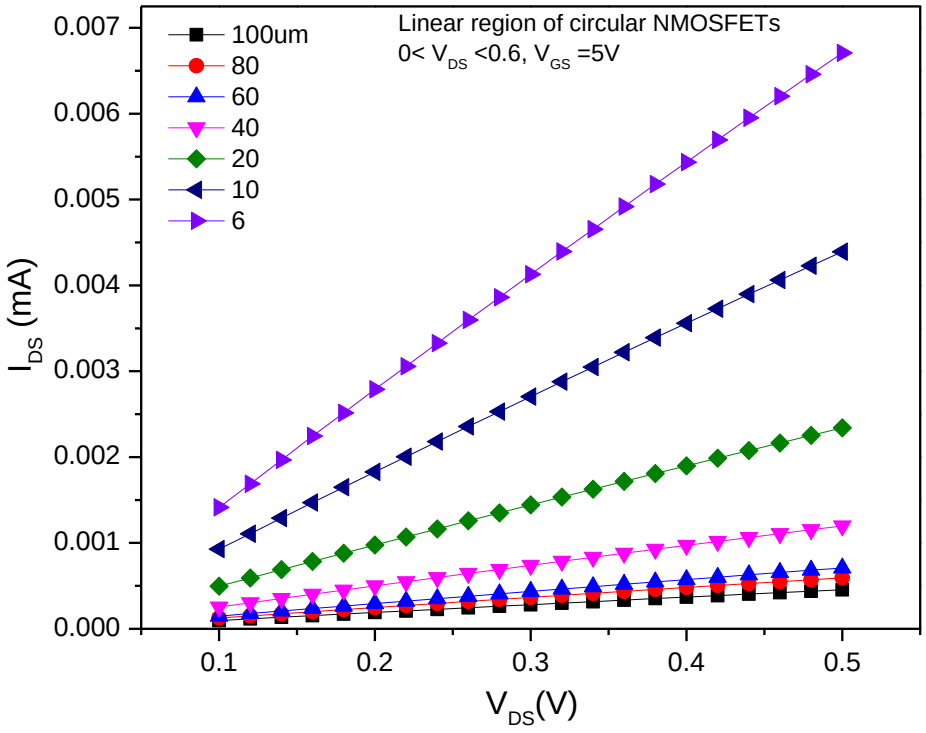

Figure 3.10.1 I_{DS}-V_{DS} characteristics of circular NMOSFETs of different channel lengths in linear region (0.1V<=V_{DS}<=0.5V) at V_{GS} = 5V.

The inverse of the slope of the output characteristics in linear region gives the on state resistance of transistors R_{ON}. The value of V_D is usually small and hence if the square of V_D term is neglected in the above equation, R_{ON} can be determined to be,

$$R_{ON} = \frac{L}{\mu_P Z C_i (V_G - V_T)}$$

As can be inferred from the above equation for R_{ON}, the value of μ_P, Z and C_i being constant, the value of R_{ON} is dependent on channel length L only. Hence, the inverse of slope of above linear region of I_D -V_D plot is plotted against the channel length as shown in figure below.

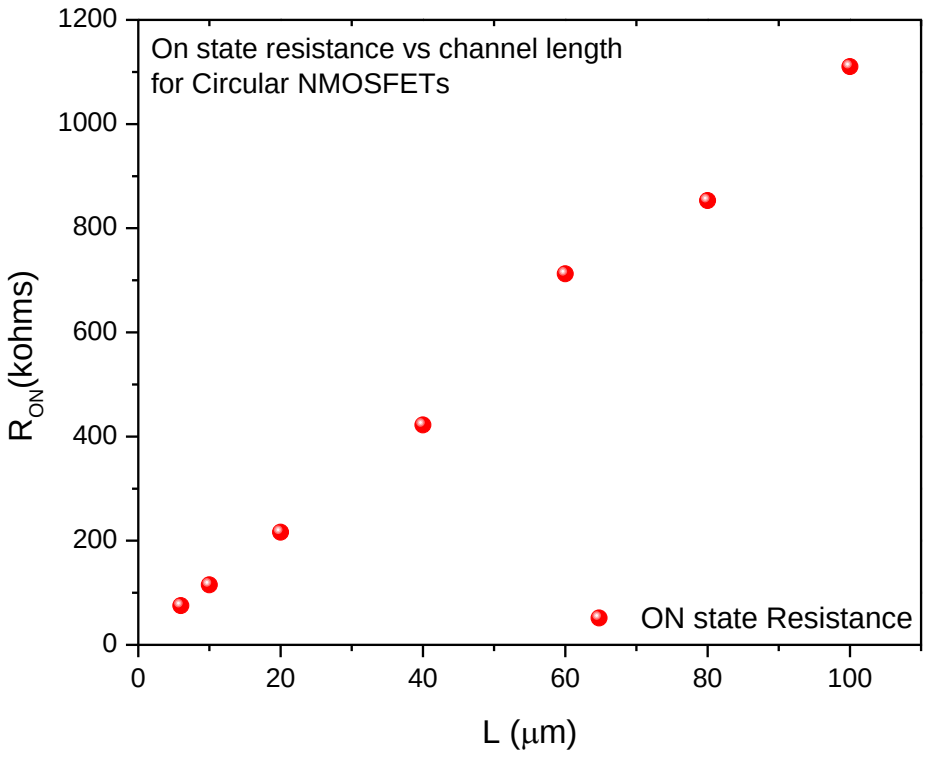

Figure 3.10.2 R_{ON} vs. L plot of circular NMOSFETs for different channel lengths in linear region (0.1V<=V_{DS}<=0.5V) at V_{GS} = 5V.

The value of the R_{ON} was calculated and has been tabulated as below. The value of R_{ON} is seen to increase linearly with increase in gate channel length as expected from the relationship between R_{ON} and L from the equation.

Table 3.10.1Table of R_{ON} at different channel lengths calculated from linear region of circular NMOSFET I_{DS} vs. V_{GS} plot.

Channel Length, L (μm)	ON State Resistance of circular NMOS, R_{ON} (kohms)
100	1110.42524
80	852.95584
60	712.35162
40	422.19625
20	216.17335
10	115.09857
6	75.31636

3.11 Failure Analysis

The three n-type Si wafers were used to fabricate PMOS devices. As mentioned earlier, PMOS wafer processing involves an extra processing step in which a 100nm thick Si_3N_4 layer is deposited and then on top of it a 700nm thick SiO_2 ILD layer is grown. In case of NMOS wafers a direct growth of ILD of thickness 800nm is done by PECVD process. The purpose of this nitride layer in case of PMOS wafers is to prevent the diffusion of Boron into SiO_2.

During testing, none of the PMOS wafers produced any I_D-V_D characteristics, even though we were able to extract C-V characteristics. So destructive testing was performed on one of the PMOS wafers to understand the reason behind this. The wafer was broken along the linear PMOSFET devices of one of the dies in order to get a cross-sectional view of those devices. The cross-section was then analyzed under Secondary Electron Microscope (SEM).

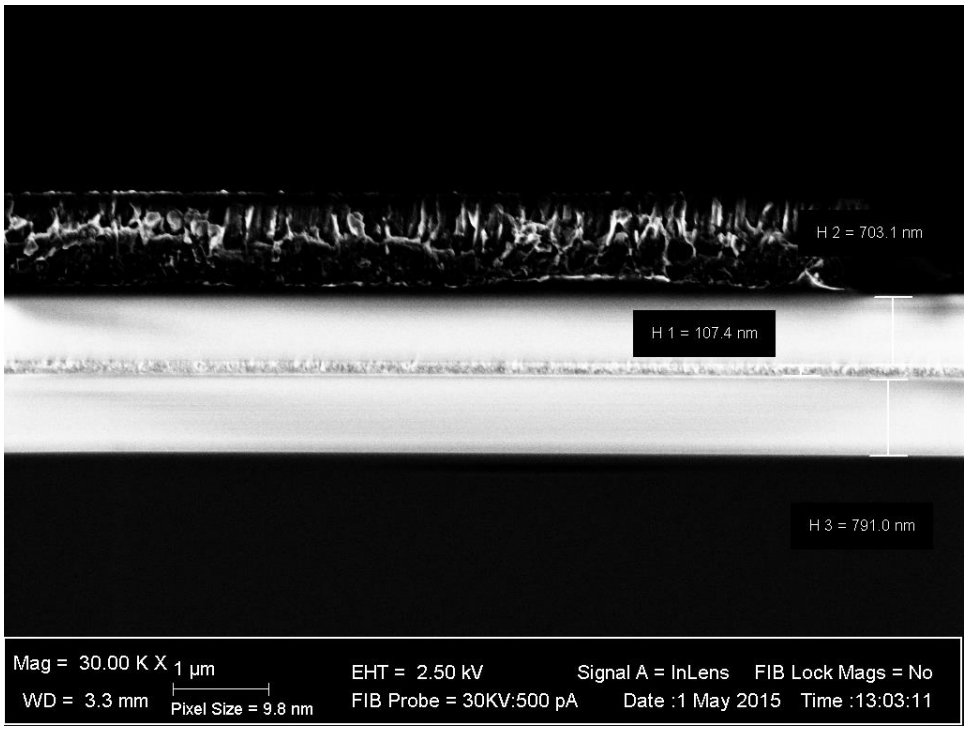

Figure 3.11.1 SEM image of the Cross-section of a linear PMOSFET with thickness of various layers indicated- ~703nm ILD oxide layer, ~107nm thick Si_3N_4 on top of ~791nm oxide layer.

As shown in Figure 3.11.1, the first cross-sectional image shows the PECVD grown ~107nm (100nm) thick Si_3N_4 and ~703nm (700nm) thick ILD oxide layer on top of ~791nm (800nm)

thick field oxide. The ILD and Si_3N_4 were removed from the active region prior to metallization by RIE etching. In which the etch time was determined by calculating the highest thickness of ILD and adding 20% extra thickness and dividing this thickness by the etch rate of 90nm/min for SiO_2 and 60nm/min for Si_3N_4.

But as it was discovered, it can be seen from Figure 3.11.2, the nitride layer never got etched. Hence it prevented good contact to the source and drain region from the metal deposited on top, which explains no I-V output characteristics from the PMOS wafers. The probable reason for this might be the RIE etch time was not enough to etch the nitride layer. It is always preferable to over-etch while etching the ILD and nitride layer as under-etch might result in a thin un-etched Si_3N_4 layer on top may prevent good contact, but few nm over-etch into source and drain region doesn't result in any harm.

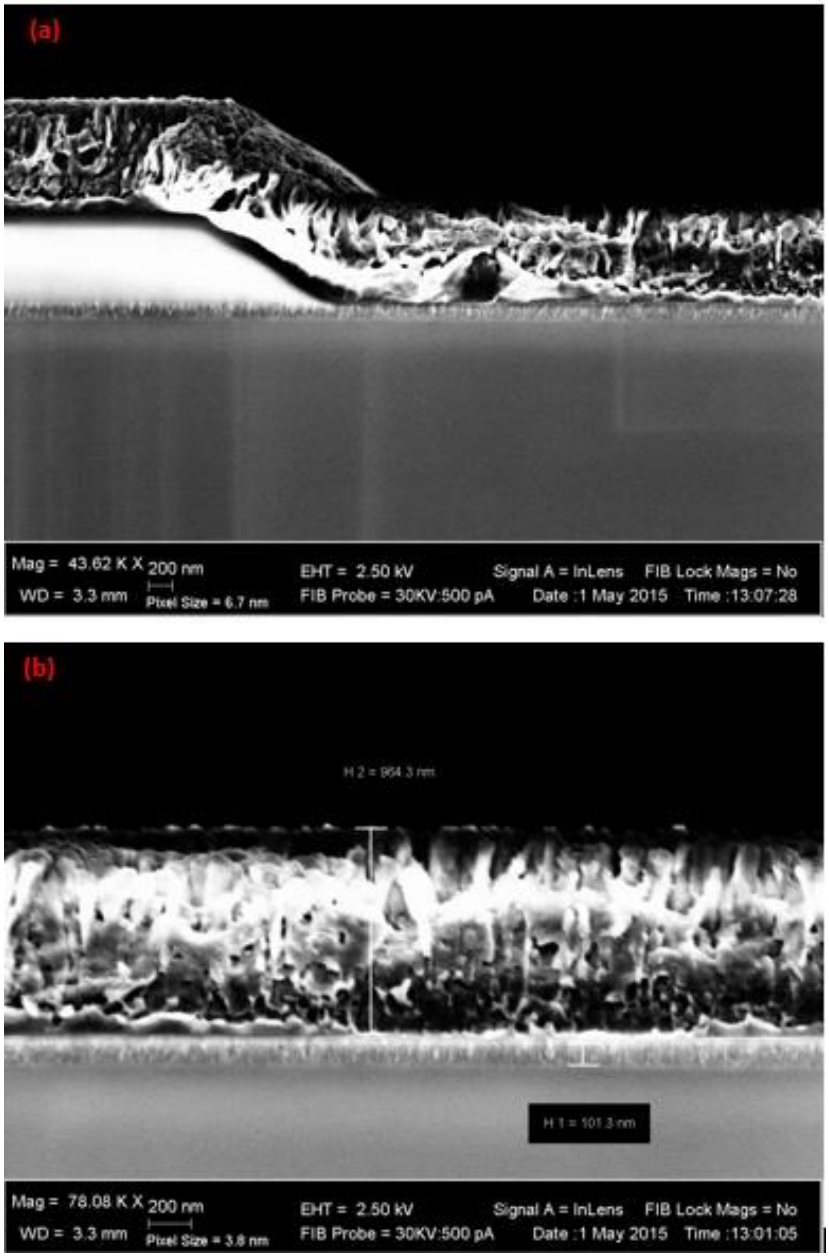

Figure 3.11.2 SEM images of the Cross-section of a linear PMOSFET (a) showing the S/D region on the right with a continuous Si_3N_4 layer underneath, (b) a magnified image of the S/D region with ~964nm thick Al electrode on top of un-etched ~101nm thick Si_3N_4 layer.

Also ILD etching process is followed by a BOE cleaning process to remove any residual ILD remaining on the wafers. It helped to remove the ILD, which is why no ILD can be seen on top of the un-etched Si_3N_4 layer. But BOE is not very effective in removing the Si_3N_4 layer, hence even though the BOE etching process was done, the un-etched nitride layer remained intact in the source and drain region prior to metallization.

4. Summary and Conclusions

In this IC fabrication lab course, we learned the fundamental principles of semiconductor device manufacturing as well as having extensive hands-on experience in fabricating these device in a cleanroom environment. Through multiple processes, including thermal oxidation, photolithography, CVD, PVD, RIE, and ion implantation, we successfully fabricated different types of devices on 5-inch wafers.

The C-V measurements for both PMOS and NMOS capacitors showed fairly good results in both low and high frequency regimes. The accumulation, depletion, flat band and inversion regions showed quite close to ideal characteristics. The oxide thickness, oxide capacitance and fixed charges in oxide were calculated from the characteristics. The PMOS oxide thickness was found to be close to 112nm, oxide capacitance 155pF, fixed oxide charges 4.4 x 10^{10} cm^{-2}. Depletion capacitance was found to be nearly 50.3pF with the maximum depletion width of ~1µm and acceptor doping concentration to be 1.23 x 10^{15} cm^{-3}. The threshold voltage of PMOS capacitor was found to be -1.6V which suggests that the PMOS capacitors were Enhancement mode and the inversion region is induced by application of negative gate voltage. The NMOS oxide thickness was found to be an average of 111 nm for one wafer and 220 nm for another wafer. As the thickness of the oxide is calculated from the measured capacitance it is believed that there is an unaccounted for effect reducing the capacitance of the wafer to give this result. The anomalous wafer was found to have an oxide capacitance of 79 pF while the wafer in line with expectations had an average capacitance of 155pF. The depletion capacitance was found to be 46 pF on average and the maximum depletion width was found to be 1.15 µm. The threshold voltage of the NMOS wafers was found to be in the range from -0.75 V to 0.36 V. The dopant concentration of the NMOS wafers was found to be 9.2*10^{16} cm^{-3}, and the fixed oxide charge was found to vary from .209 to -.025 mC/m^2.

The effect of pad dimensions on contact resistivity can be seen in table xx. This is most likely due to the current crowding phenomenon where a lot of the current flows more towards the edge of the pad, and goes to zero as the contact pad gets larger. Since we tested 4 different nMOS wafers, we also found the average and the standard deviation among the wafers was between 0.04 to 1.19. The standard deviation was very small, which also tells us that there was uniformity across our nMOS wafer fabrication. . The Kelvin structure is a much better way of determining the contact resistance than the transmission line method, which is why our results are more ideal and consistent. The results from the TLM however, are an order of magnitude different from the other structures. This is likely due to errors in data collection or testing setup.

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