Fabrication and Electical Characterization of MOSFETs

ECSE 6300: Integrated Circuit Fabrication Laboratory, Spring 2015
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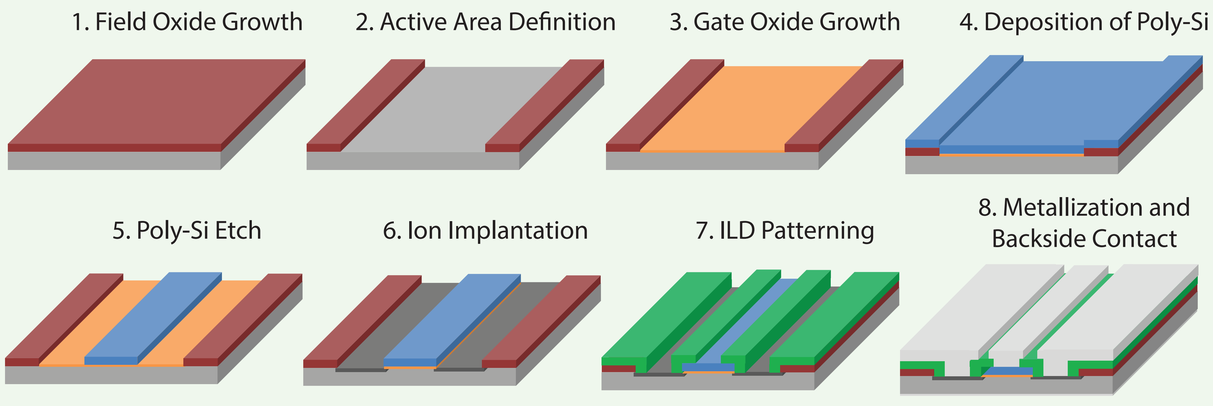
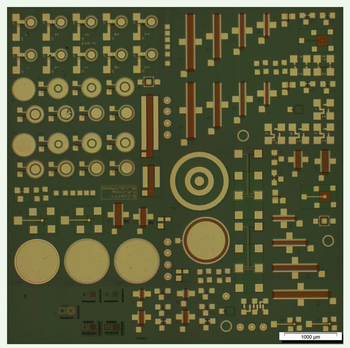
Abstract

This poster details the processes that were used in the fabrication and characterization of devices on n-type and p-type wafers. This was a semester long project and our pertinent results and extracted data can be seen below.

The fabrication processes include oxidation, ion implantation, photolithography, etching, film deposition and metallization. These are the most basic steps needed to fabricate working devices; recent technology requires much more precision and extra steps like epitaxial layer growth for advanced CMOSes. The following devices were characterized: circular MOSFETS, rectangular MOSFETS, capacitors, Van der Pauw structures, Kelvin Structure, and transmission lines.

MOSFET Fabrication

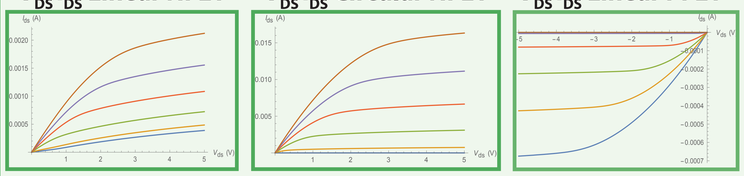




Finished Die

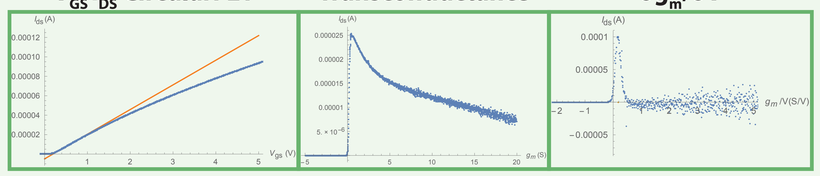
Electrical Characterization

V_{DS} I_{DS} Linear NFET | **V_{DS} I_{DS} Circular NFET** | **V_{DS} I_{DS} Linear PFET**



As can be seen in the above graphs, the linear NFET has significantly more leakage current than both the circular PFET and the linear PFET. This is due oxide charge

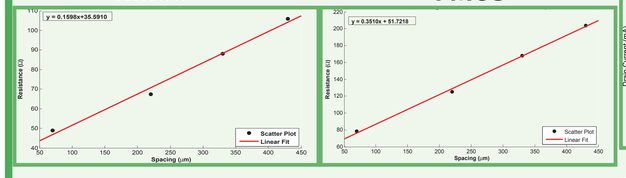
V_{GS} I_{DS} CircularFET | **Transconductance** | **$\delta g_m/\delta V$**



V_{gs} data was used for extracting V_{th} and g_m. V_{th} extraction was done both with fit to max g_m with extrapolation and with max δg_m.(0.20V vs 0.19V). Mobility and unknown W/L ratios can be found with $g_m = \mu_n C_{ox} W/L$.

Transmission line measurement

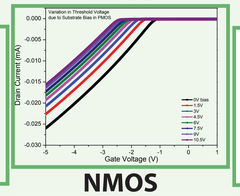
NMOS | **PMOS**



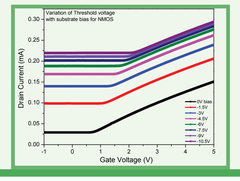
nMOS Contact resistance =17.75Ω,
Sheet resistance =283.6Ω/square
pMOS Contact resistance = 25.86Ω,
Sheet resistance = 160.10Ω/square

Substrate Bias Threshold

PMOS

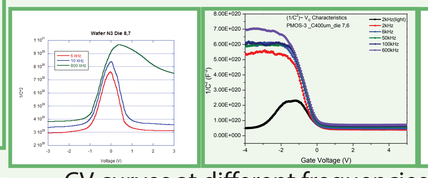


NMOS



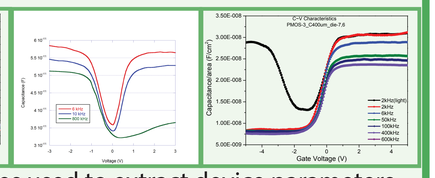
$1/C^2$ vs Vg

NMOS | **PMOS**



CV measurement

NMOS | **PMOS**

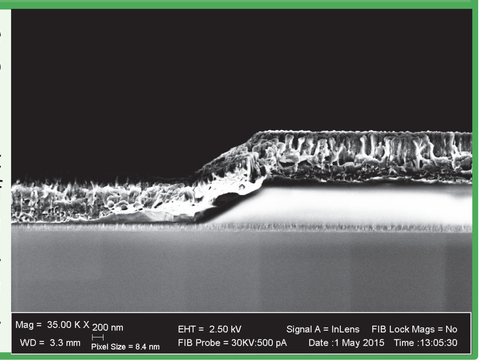


CV curves at different frequencies used to extract device parameters.
PMOS: T_{ox}=112 nm, C_{ox} = 155 pF, W = 1.03 um, V_{th} = -1.6 V, QF=7x10^{-9} C/cm^2 , C_{dep}=50.3 pF, ND = 1.23x10^{15} cm^{-3}
NMOS: T_{ox}=120 nm, C_{ox} = 78.6 pF, W = 1.05 um, V_{th} = 0.36 V, C_{dep}=49.3 pF, ND = 7.9x10^{15} cm^{-3}

PMOS Failure

The image to the right is the result of SEM imagery to investigate PMOS Failure.

When looking at the contact interface under SEM, a layer of nitride can be seen between the aluminum and silicon. This layer is roughly 100nm thick, the same as deposited.



Conclusions

- The NMOS devices worked ideally, but all of the PMOS wafers had problems. We determined that we didn't etch the oxide layer enough as seen above.
- The NFET threshold voltages were in the range of 0.15 – 0.25V, whereas the PFET was in the range of 0.65-0.75V.
- The transconductance values had an ideal correlation with the W/L ratio of the MOSFETs.
- Smaller (200um) MOS capacitors produced poorer CV characteristics as compared to larger (400um) due to their higher susceptibility to noise.